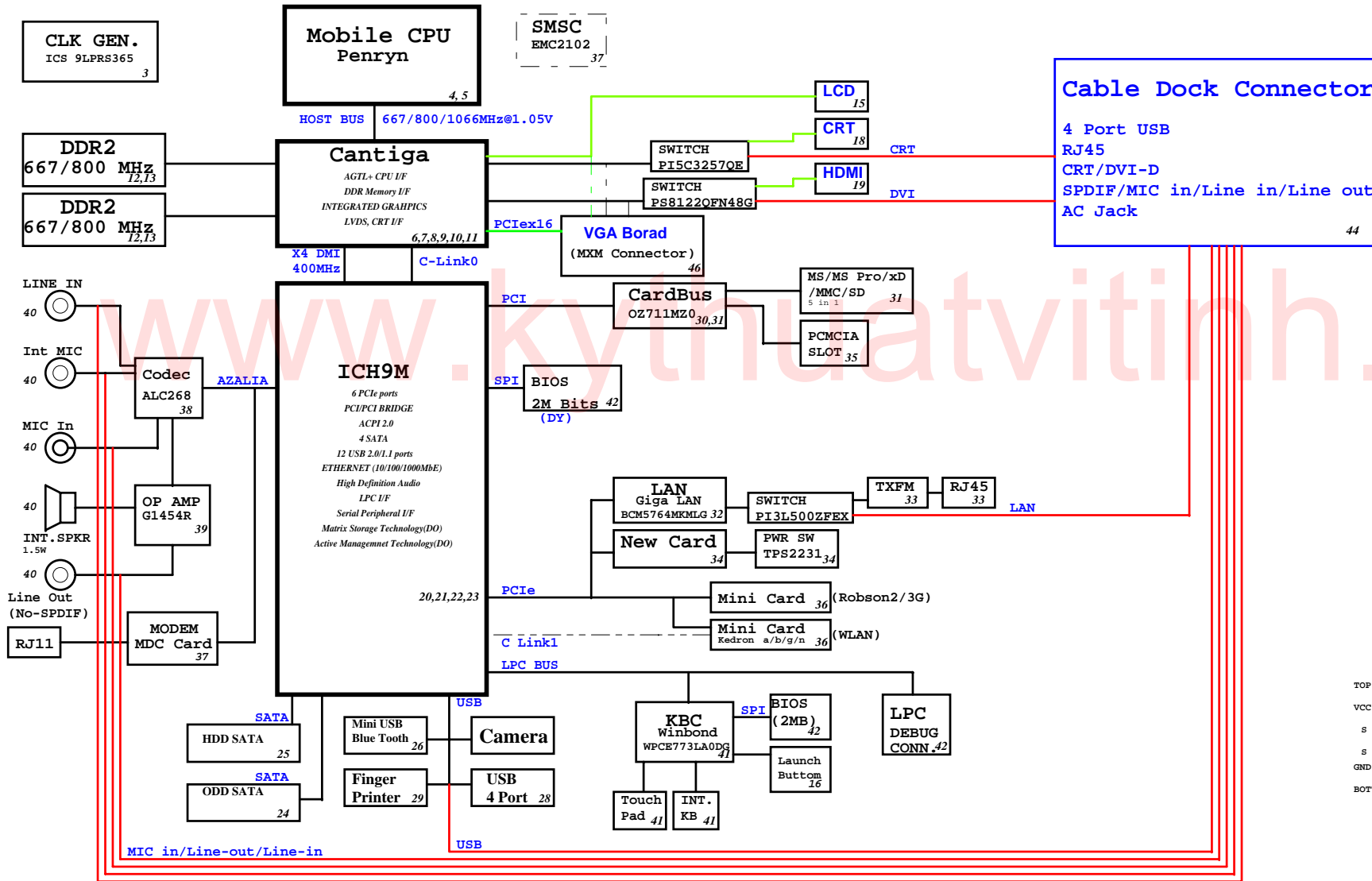


HOMA 3G Block Diagram



Project code: 91.41601.001
PCB P/N : 48.41601.011
REVISION : -1 08204

SYSTEM DC/DC TPS51125		50
INPUTS	OUTPUTS	
DCBATOUT	5V_S5(7A)	3D3V_S5(7A)
	5V_AUX_S5	3D3V_AUX_S5
SYSTEM DC/DC TPS51124		51
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0(16A)	1D8V_S3(16A)
RT9026	52	
1.8V_S3	DDR_VREF_S3(1.2A)	
G9131	52	
3D3V_S0	2D5V_S0(300mA)	
RT9018	52	
1D8V_S3	1D5V_S0(2.5A)	
CHARGER BQ24754		54
INPUTS	OUTPUTS	
DCBATOUT	CHG_PWR	18V 6.0A
CPU DC/DC ISL6266A		49
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	0-1.3V 38A
GFX DC/DC ISL6263		53
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFXCORE	0-1.3V 6.5A

PCB STACKUP

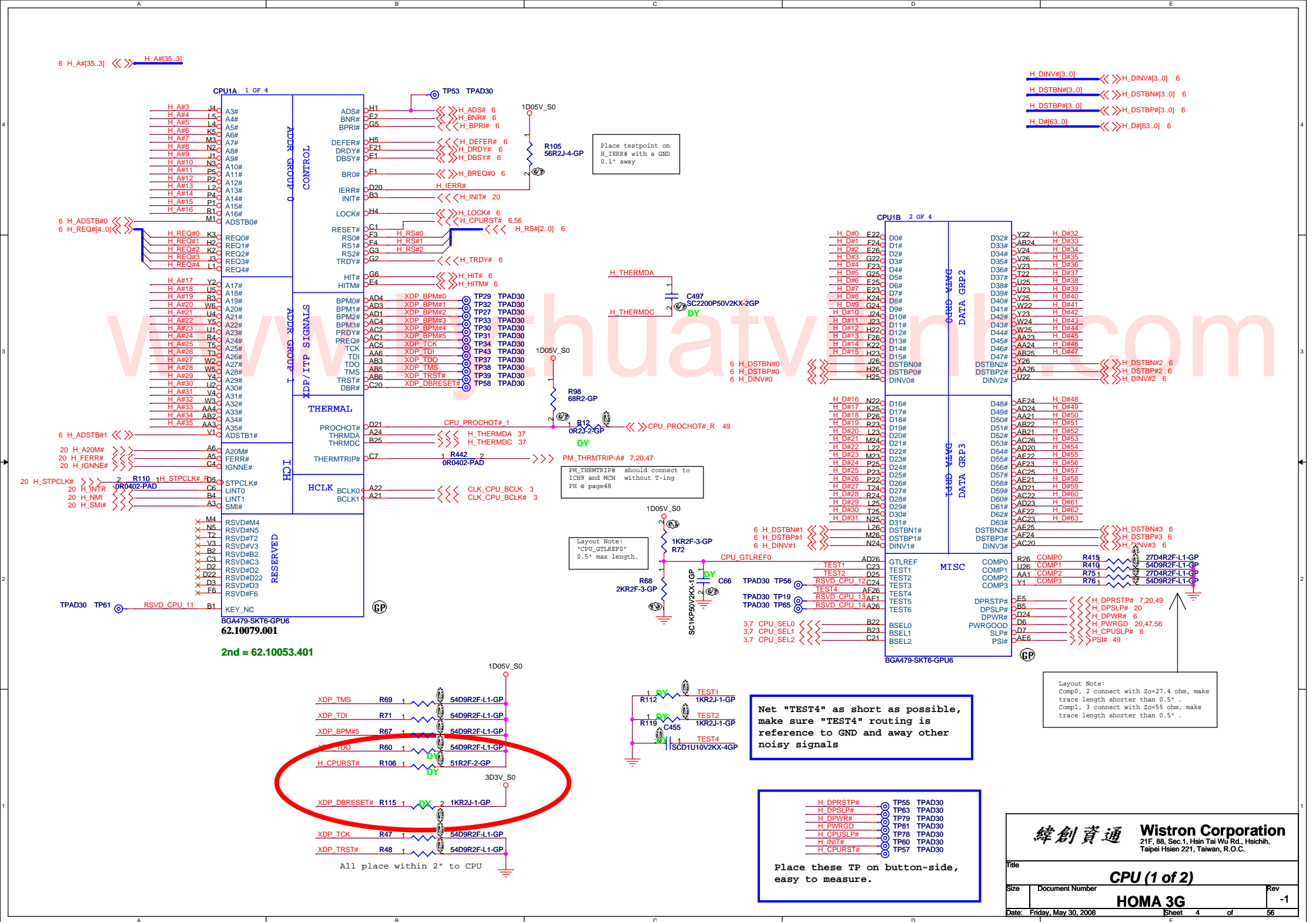
TOP	_____
VCC	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

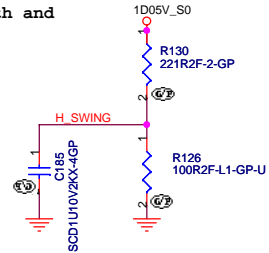
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS LPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

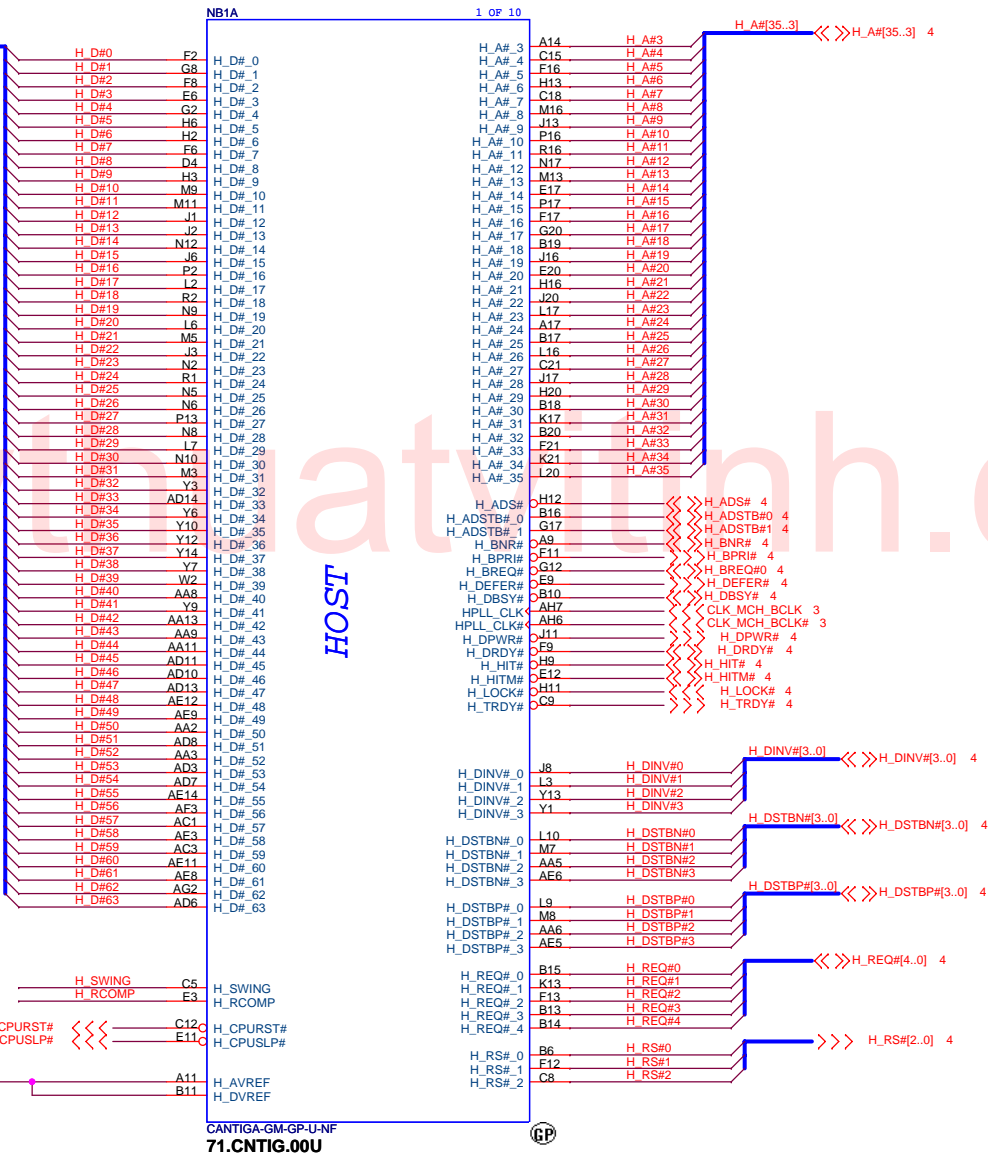
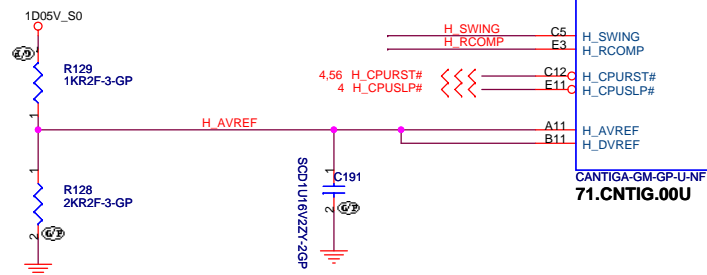


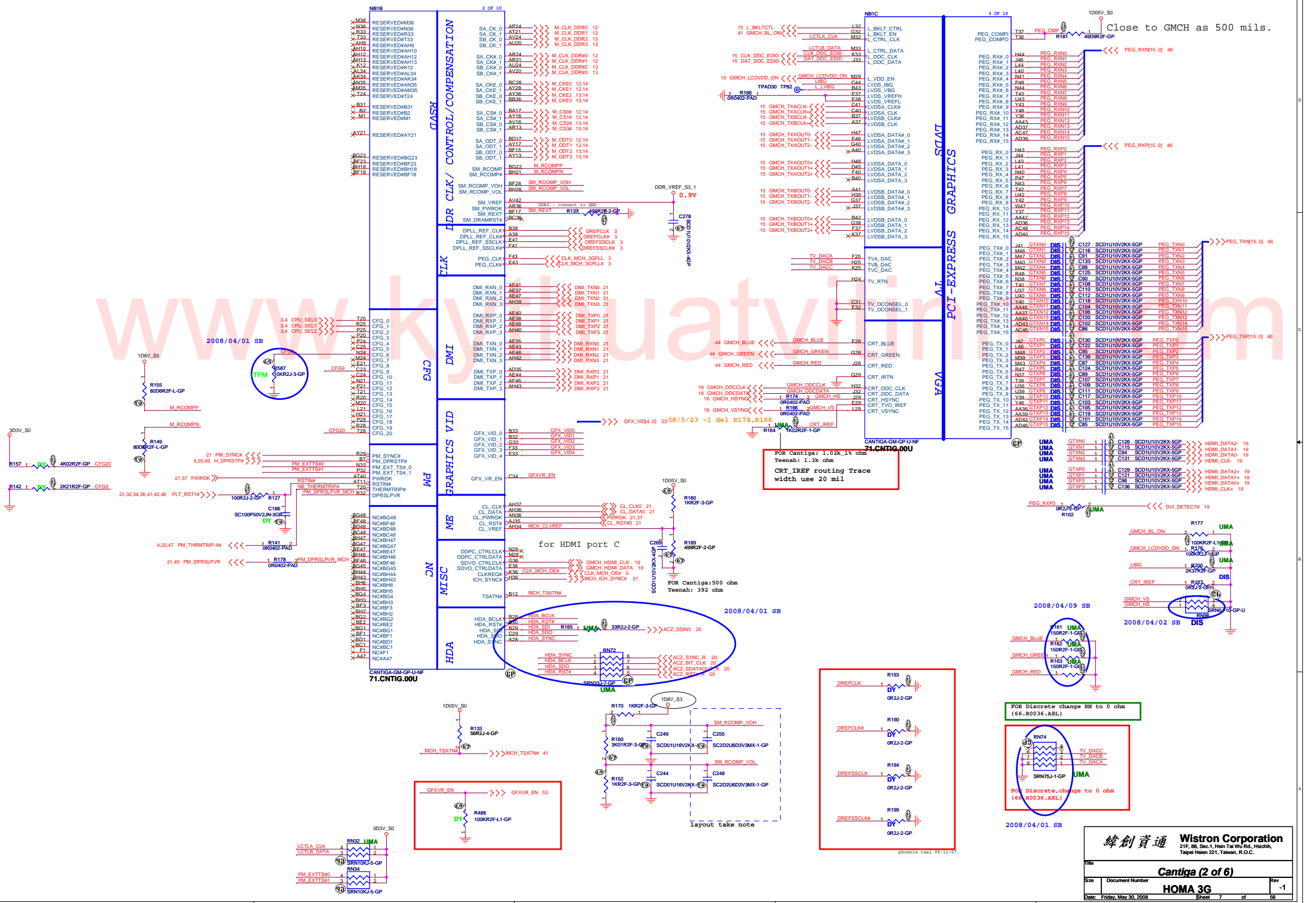
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



1
R123 24D9R2F-L-GP H RCOMP

Place them near to the chip (< 0.5")

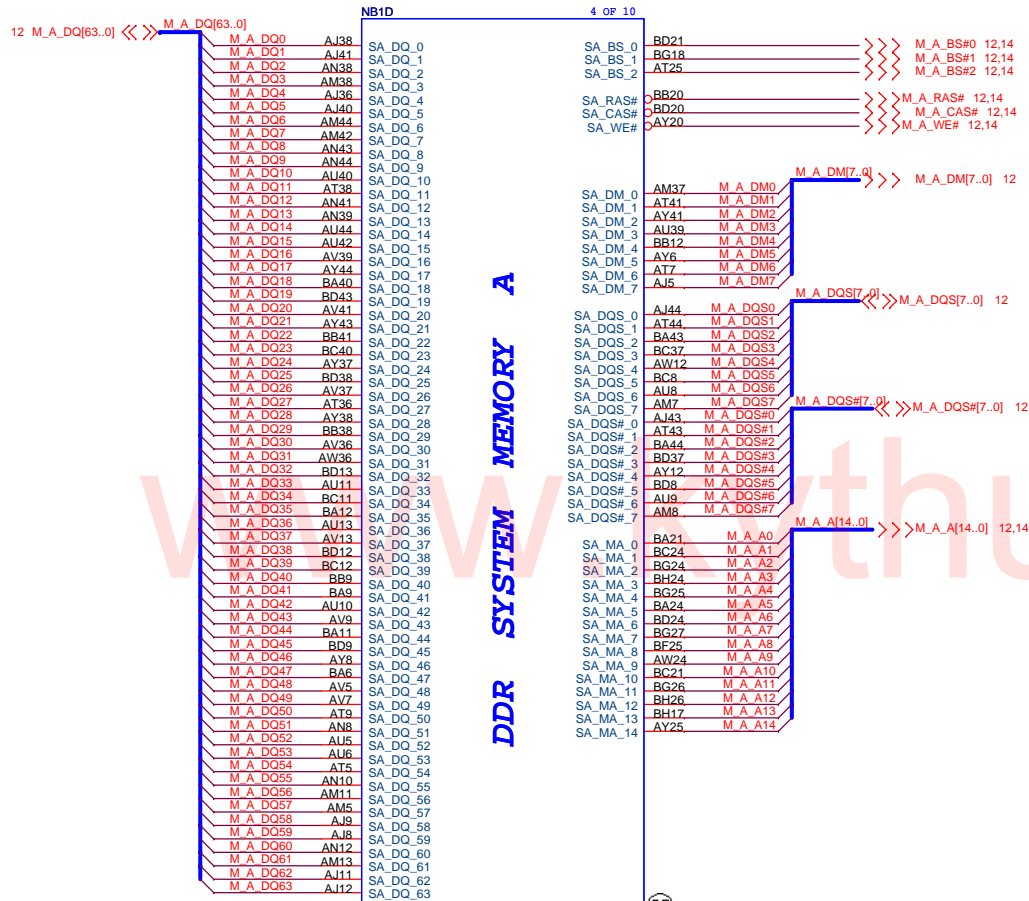




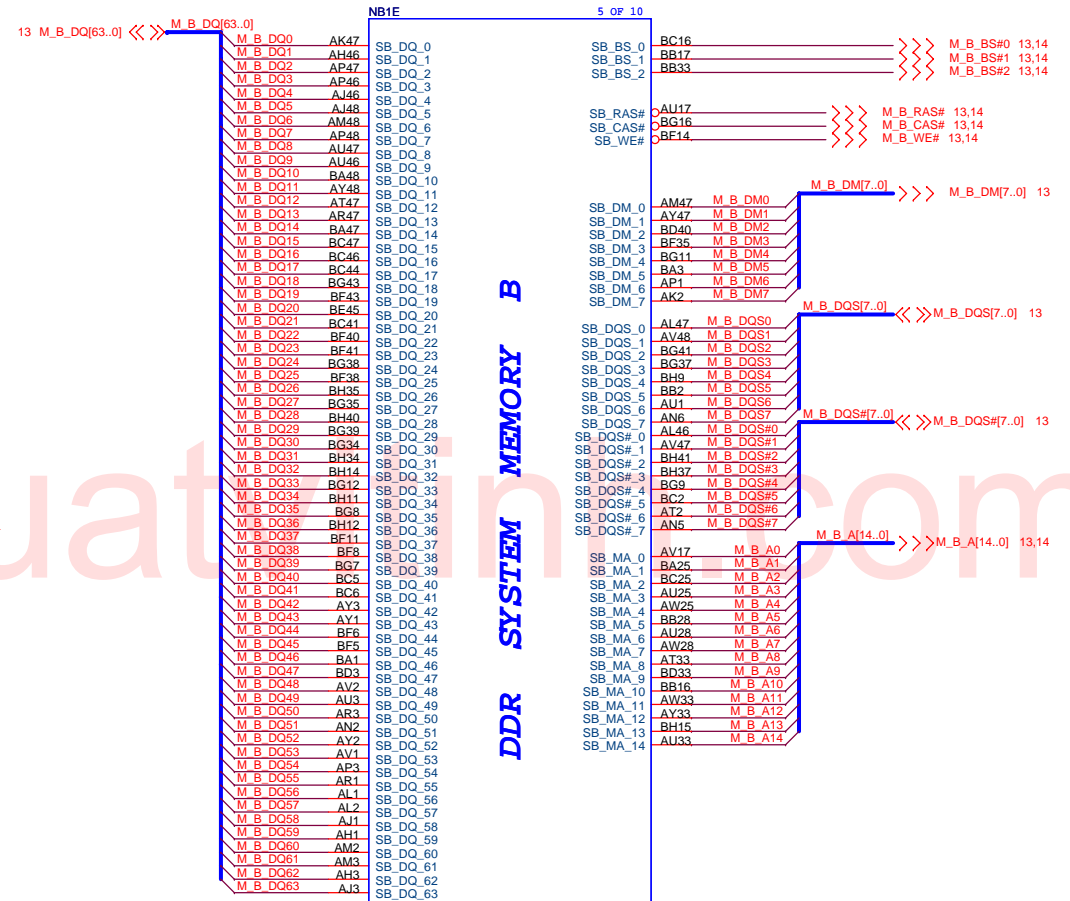
Close to GMCH as 500 mils.

FOR Cantiga: 1.02k_19 ohm
Teenah: 1.3k ohm
CRT IREF routing Trace
width use 20 mil

FOR Discrete change R1 to 0 ohm
(66.R0036.ABL)

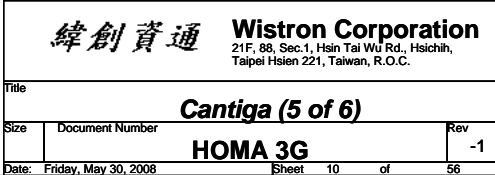


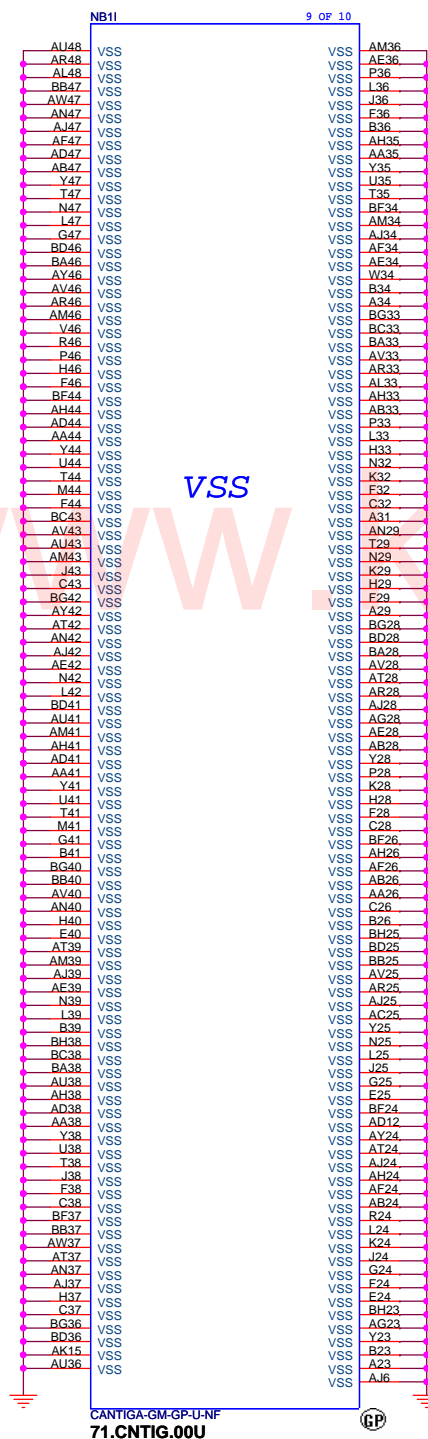
CANTIGA-GM-GP-U-NF
71.CNTIG.00U



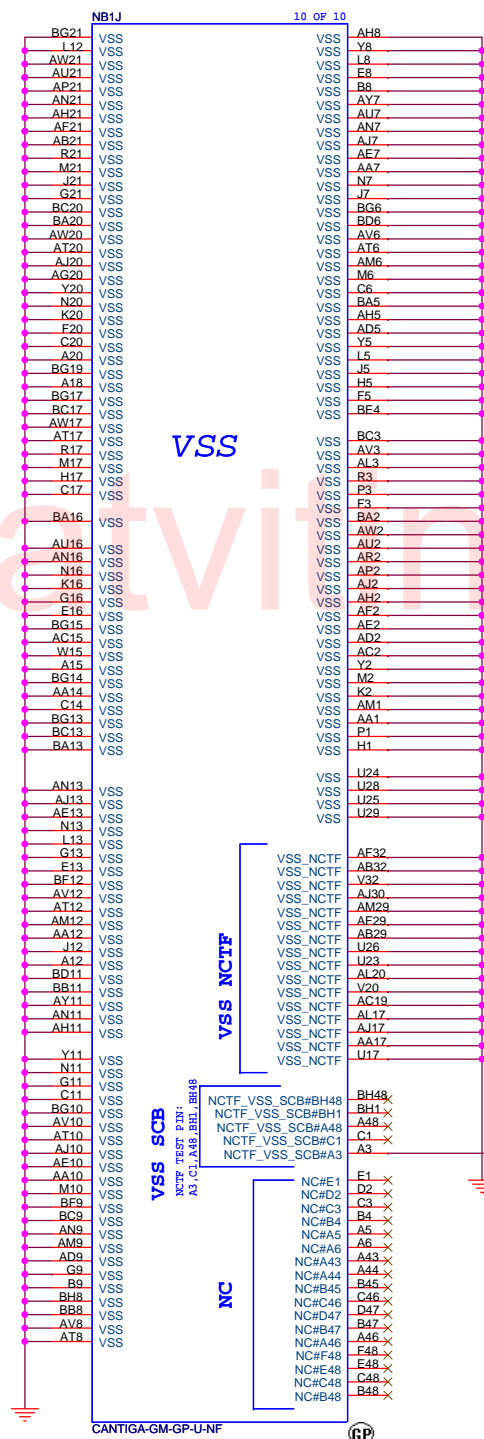
CANTIGA-GM-GP-U-NF
71.CNTIG.00U

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CANTIGA-GM-GP-U-NF
71.CNTIG.00U



CANTIGA-GM-GP-U-NF
71.CNTIG.00U



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Cantiga (6 of 6)

Rev

-1

Size

Document Number

Sheet

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of

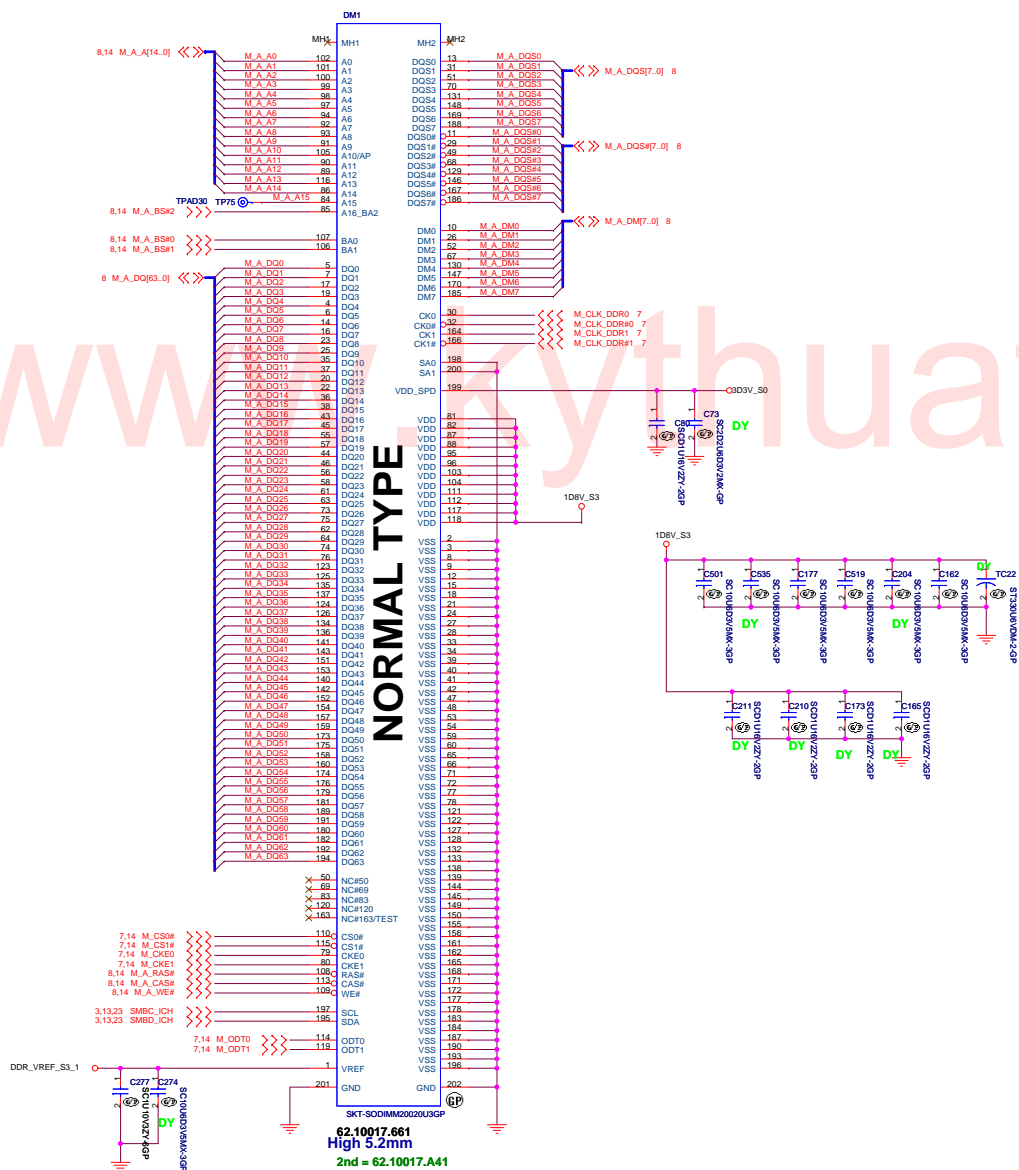
56

Date

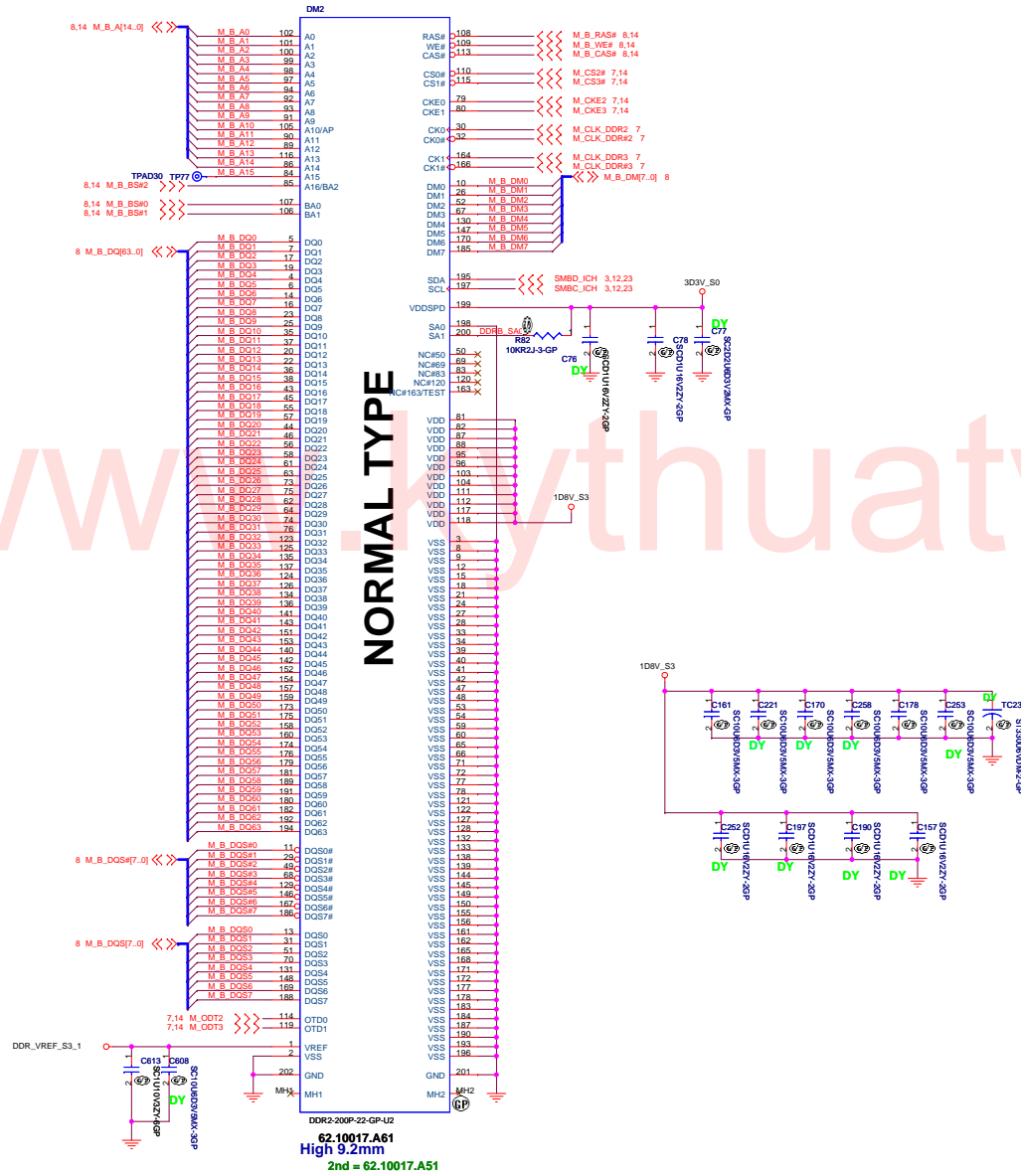
Friday, May 30, 2008

TP139 TPAD30

DDR2 SOCKET_1



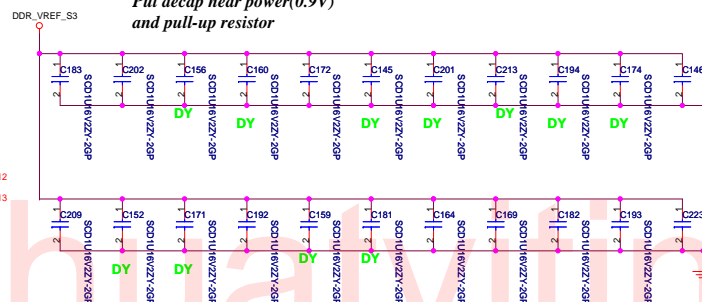
DDR2 SOCKET_2



Put decap near power(0.9V) and pull-up resistor



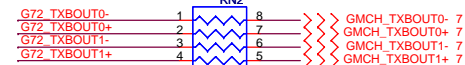
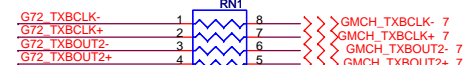
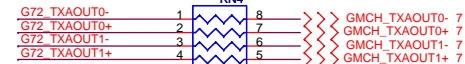
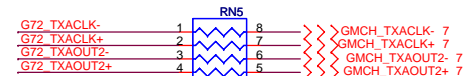
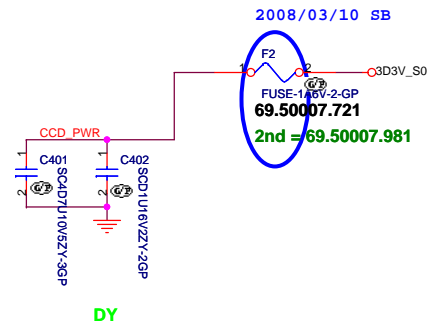
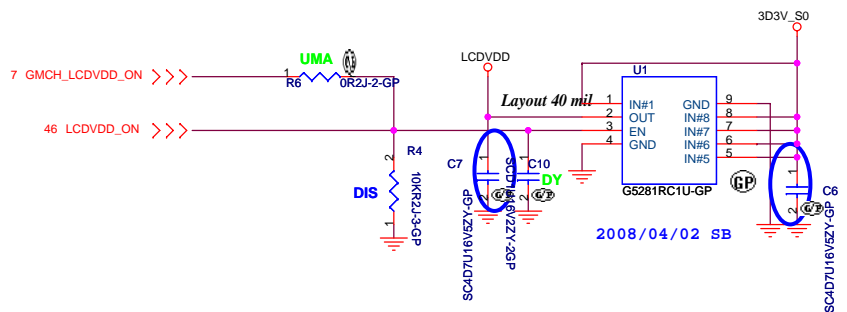
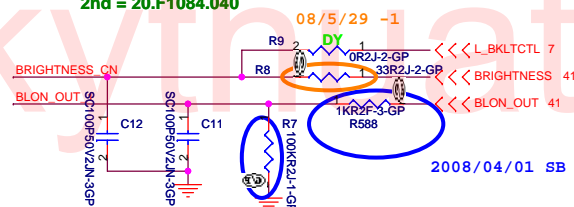
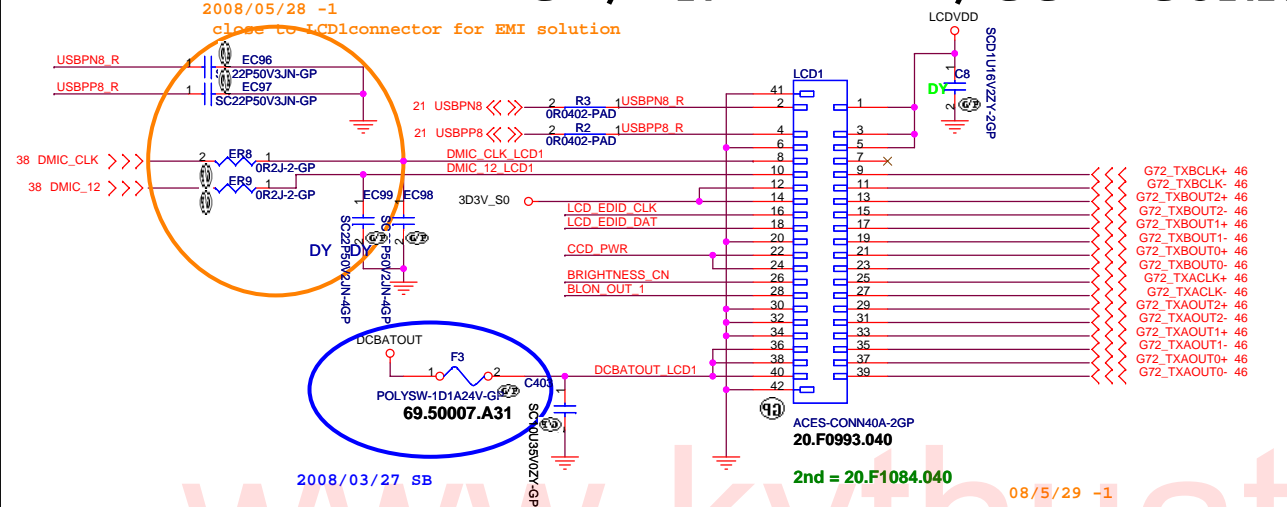
*Put decap near power(0.9V)
and pull-up resistor*



LCD/INVERTER/CCD CONN

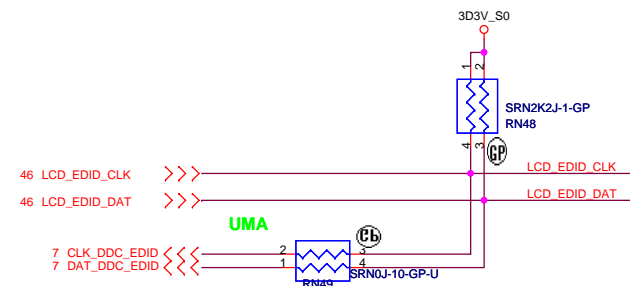
2008/05/28 -1

close to LCD1connector for EMI solution



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	GND
2	GND
3	5V
4	USB-
5	USB+

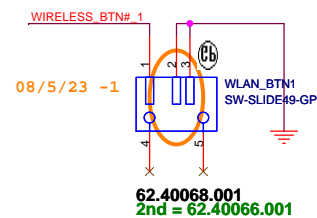


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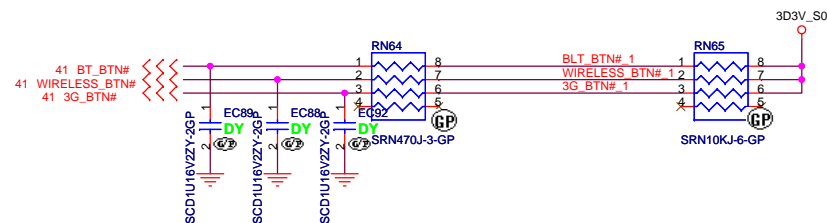
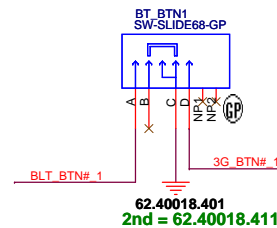
Title		LCD CONN	
Size	Document Number	HOMA 3G	
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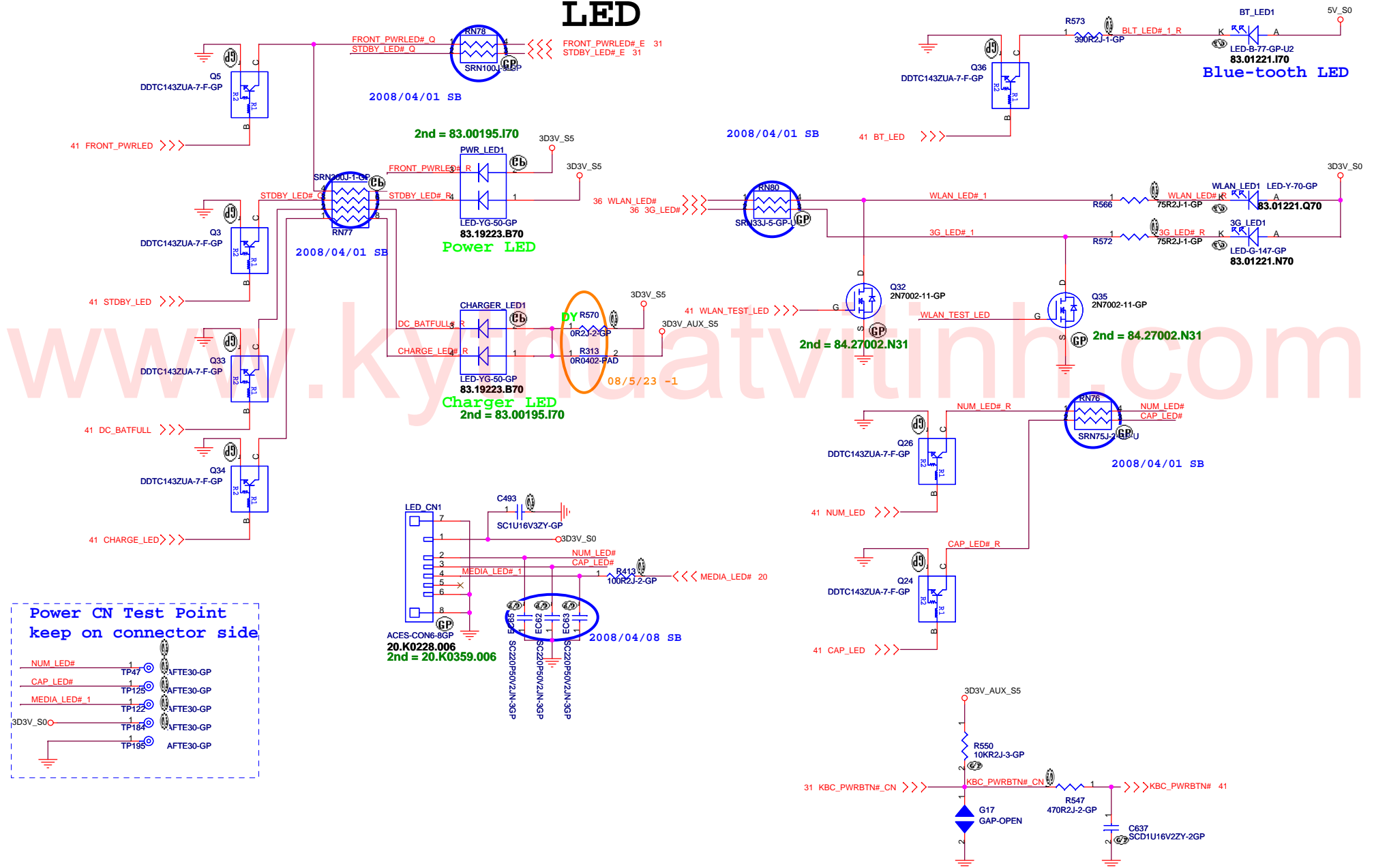
Wireless ON/OFF
Check Wireless Button left or right



BlueTooth ON/OFF



LED

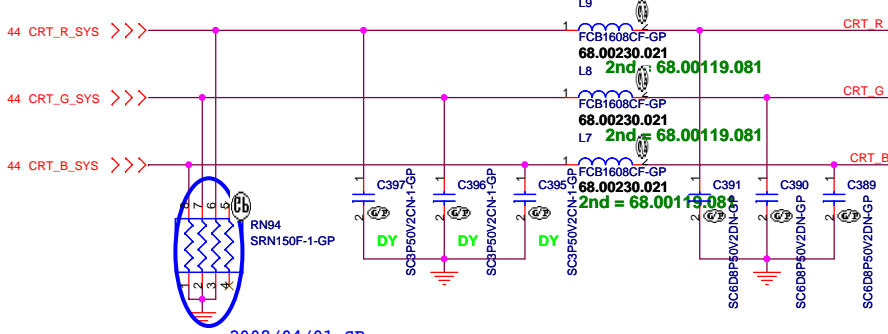


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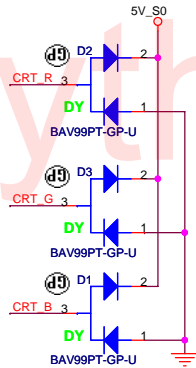
Title			
LED&POWERBD CONN			
Size	Document Number		Rev
	HOMA 3G		-1
Date:	Friday, May 30, 2008	Sheet 17 of	56

Layout Note:
Place these resistors
close to the CRT-out
connector

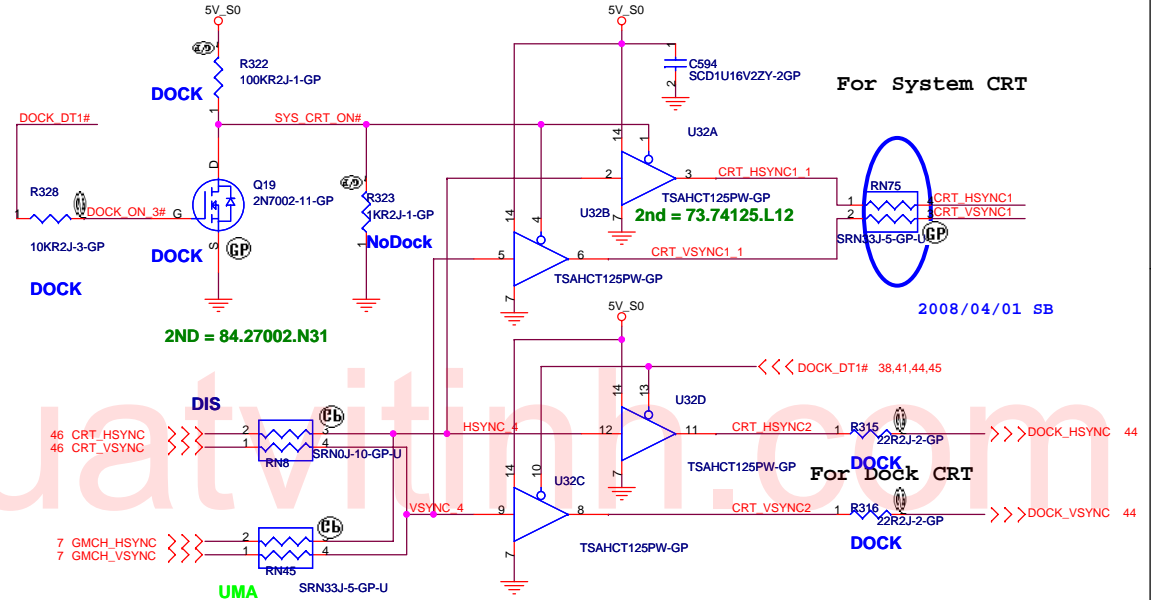
Ferrite bead impedance: 10 ohm@100MHz.



Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

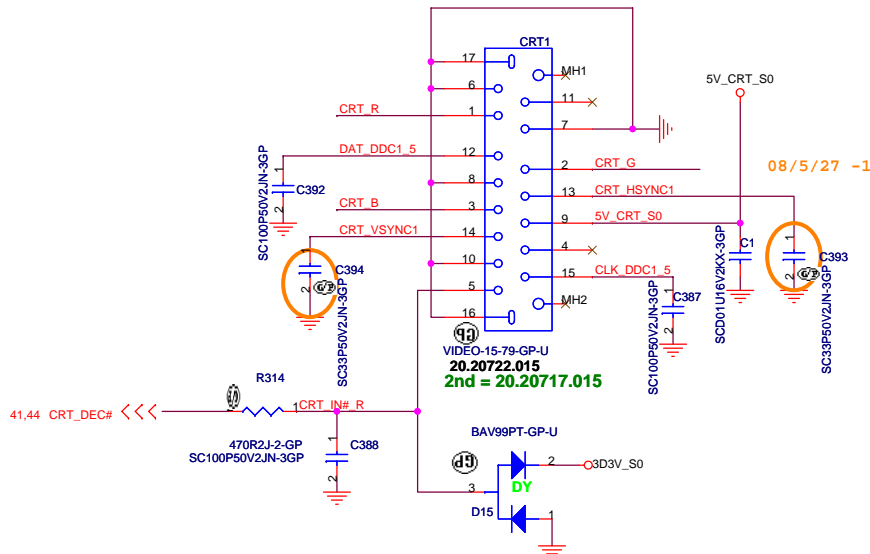


Hsync & Vsync level shift



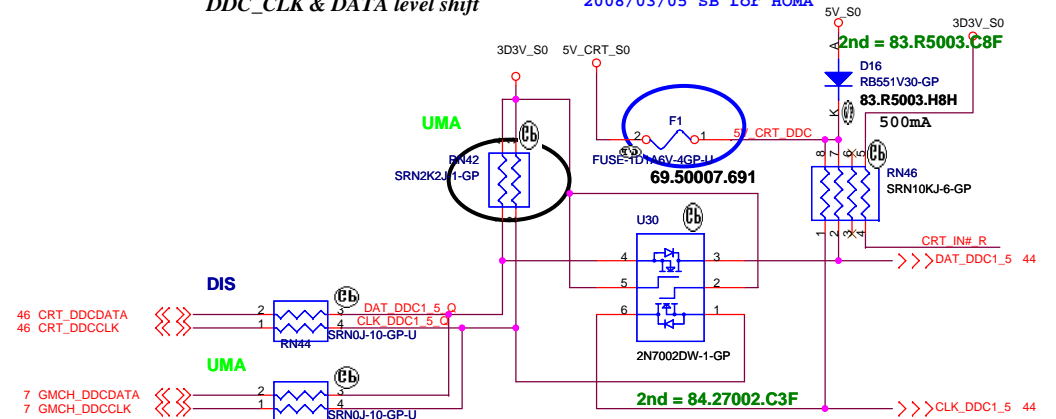
Function	DOCK_CRT_SEL#
SYSTEM	H
DOCK	L

CRT I/F & CONNECTOR



DDC_CLK & DATA level shift

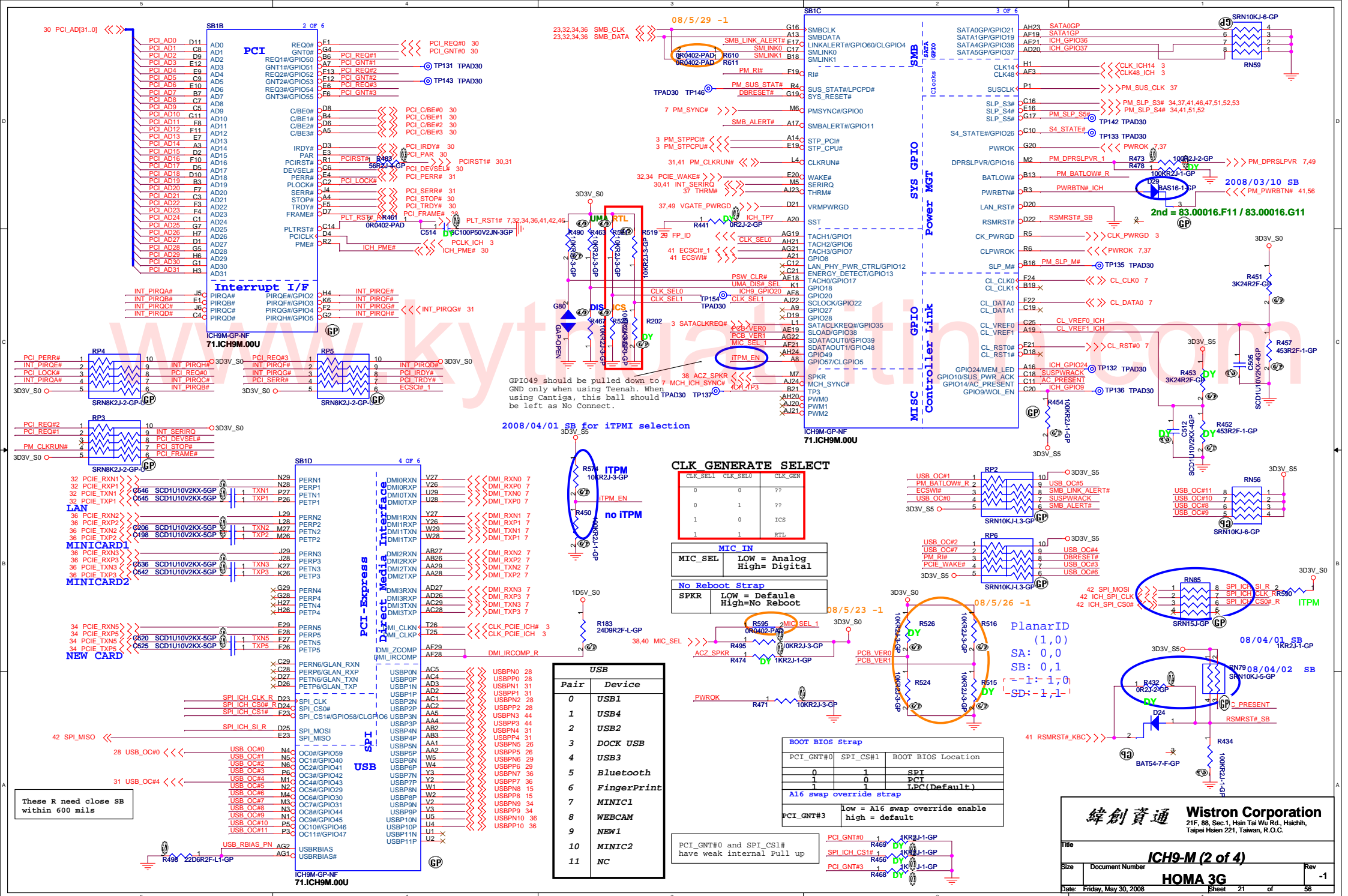
2008/03/05 SB for HOMA



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Title	CRT CONN	Rev	-1
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USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FingerPrint
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

CLK GENERATE SELECT

CLK_SEL1	CLK_SEL2	CLK_SEL3
0	0	??
0	1	??
1	0	ICS
1	1	RTL

MIC IN

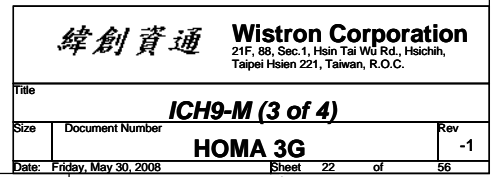
MIC_SEL	LOW = Analog High = Digital
---------	--------------------------------

No Reboot Strap

SPKR	LOW = Default High = No Reboot
------	-----------------------------------

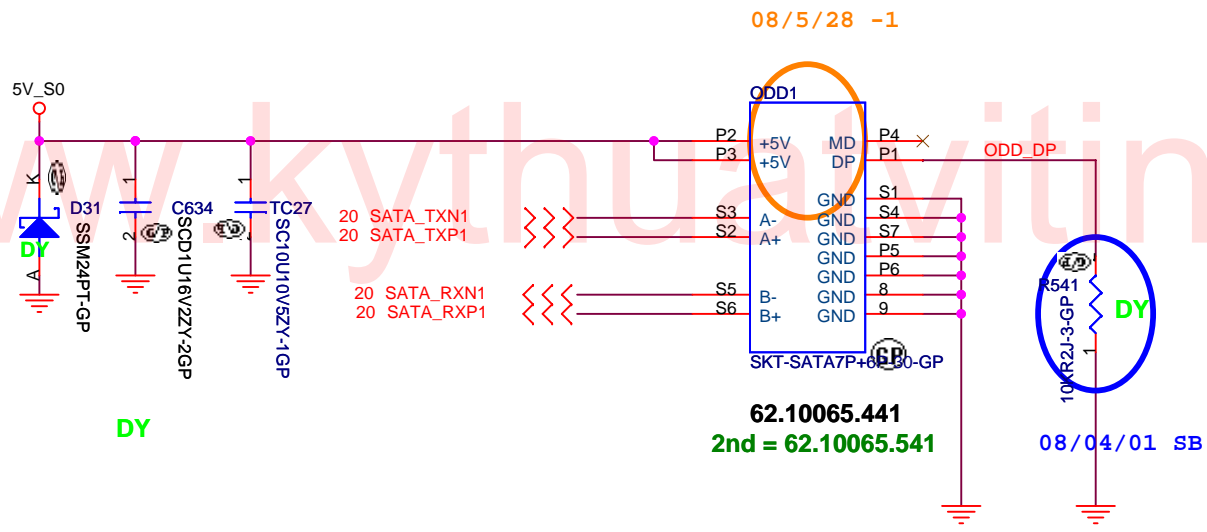
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Title	ICH9-M (2 of 4)		
Size	Document Number	HOMA 3G	Rev -1
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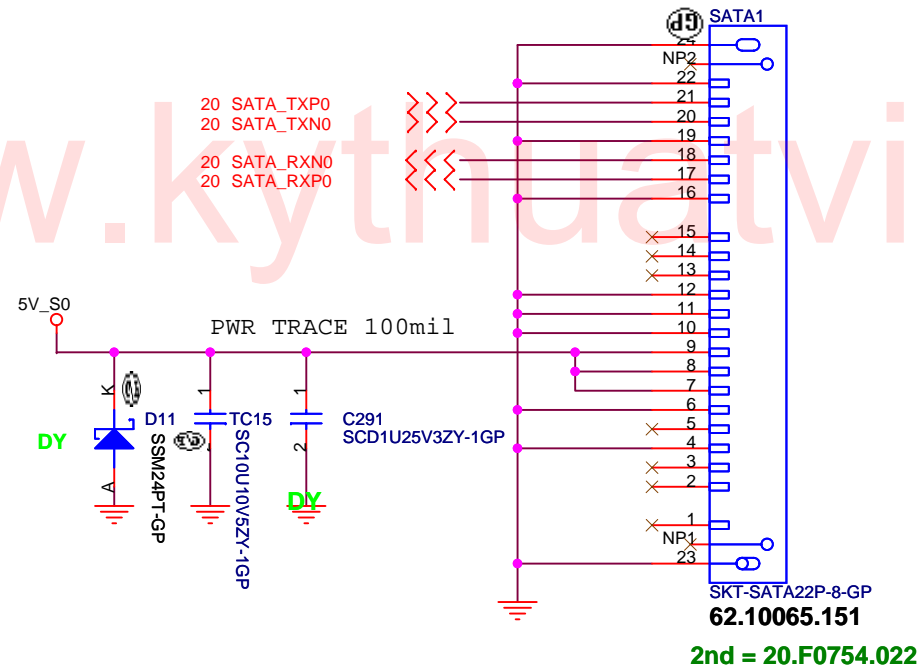




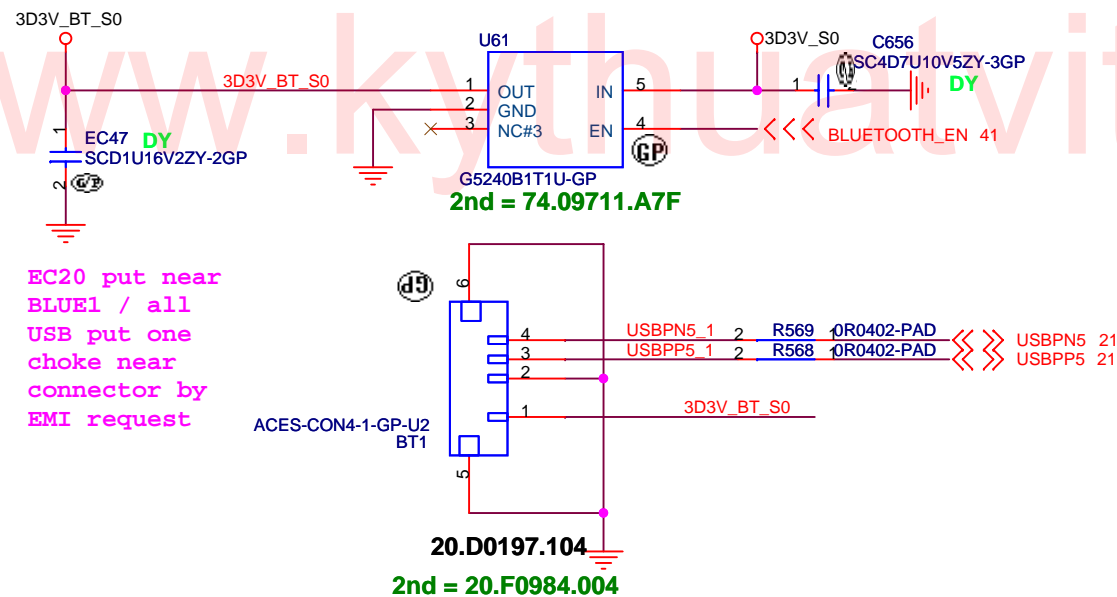
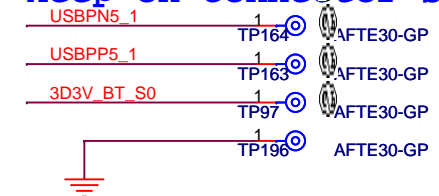
ODD Connector



SATA Connector



BT Conn. Test Point
keep on connector side



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

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Title

BLUETOOTH

Size	Document Number
------	-----------------

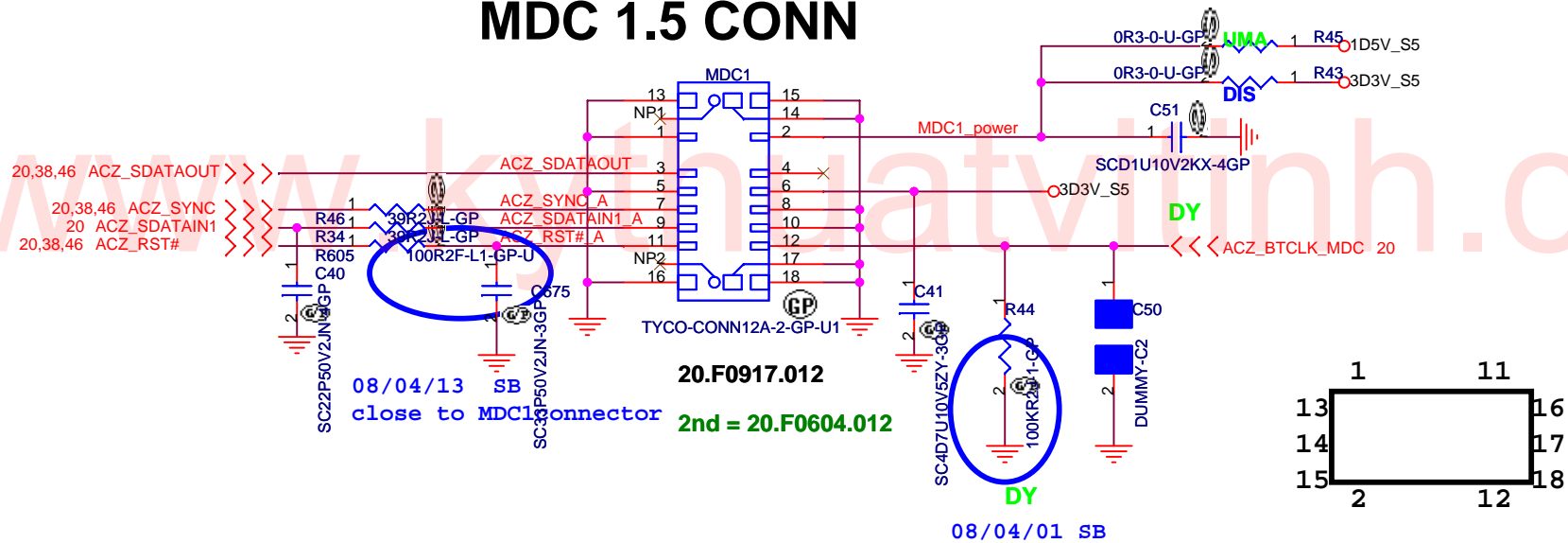
HOMA 3G

Rev	-1
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MDC 1.5 CONN



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Title

MDC

Size

Document Number

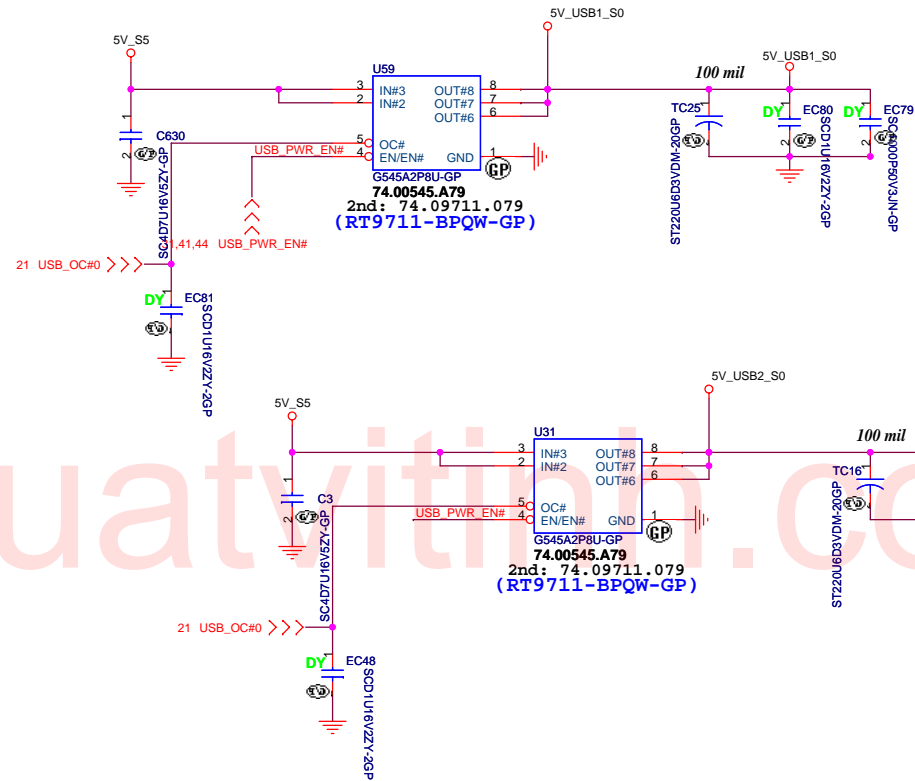
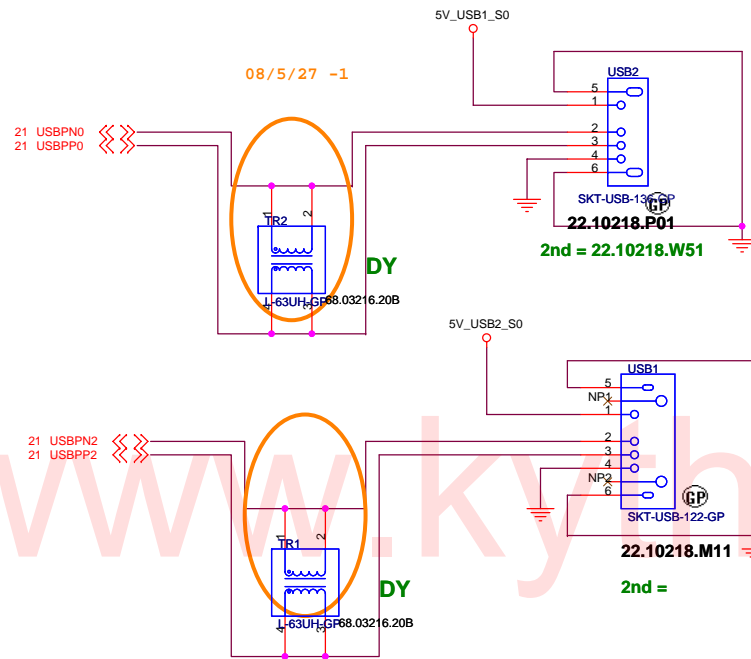
HOMA 3G

Rev

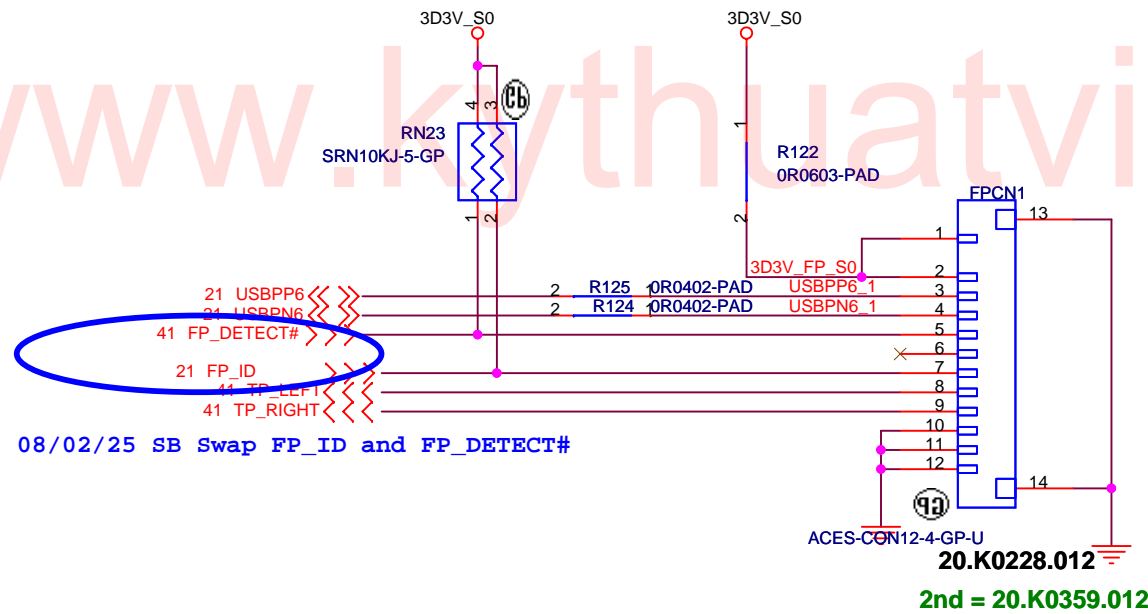
-1

Date: Friday, May 30, 2008

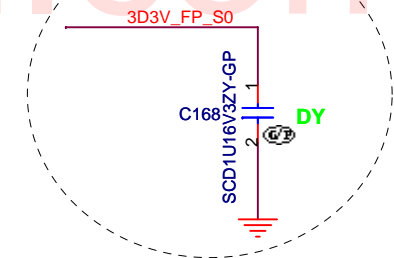
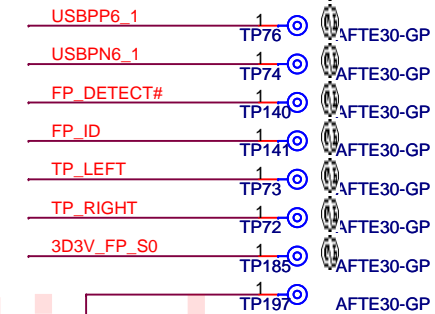
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Finger printer



FP Conn. Test Point
keep on connector side



緯創資通

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Title

Finger Printer

Size

Document Number

HOMA 3G

Rev

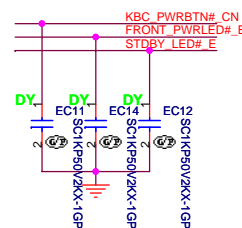
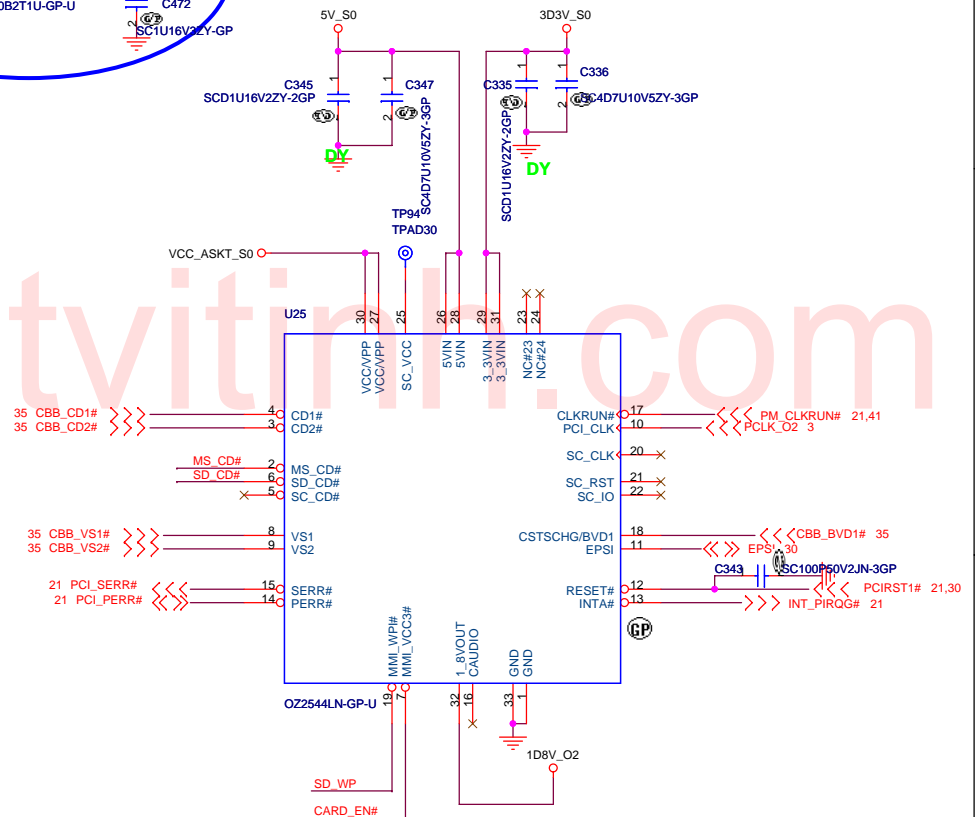
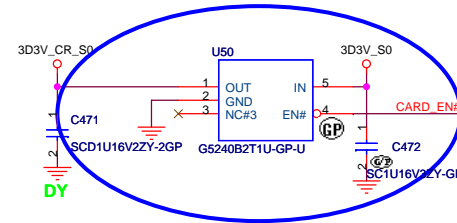
-1

Date: Friday, May 30, 2008

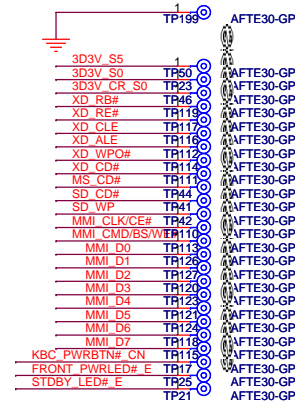
Sheet 29 of 56



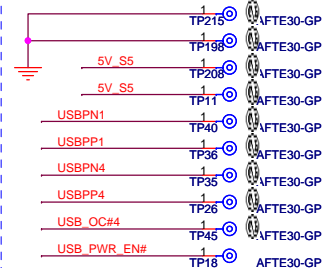
2008/04/02 SB follow 4P



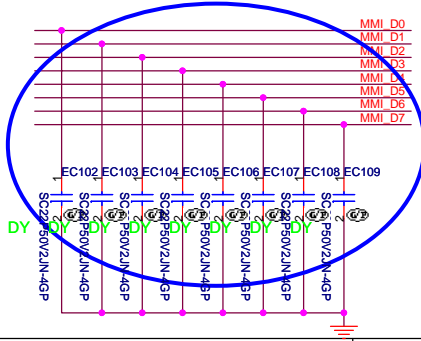
DB_CN2 Conn. Test Point
keep on connector side



DB_CN1 Conn. Test Point
keep on connector side

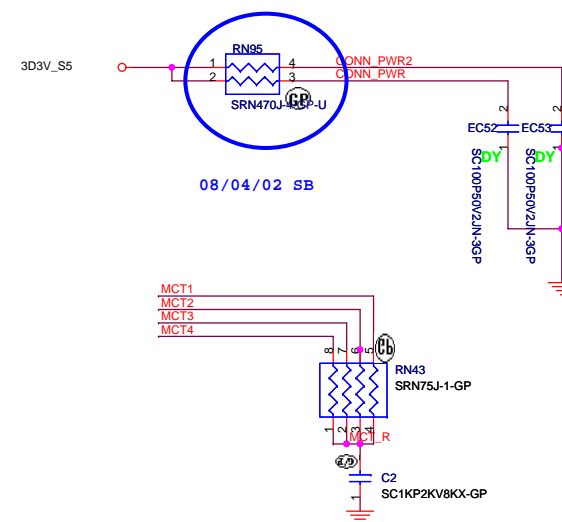
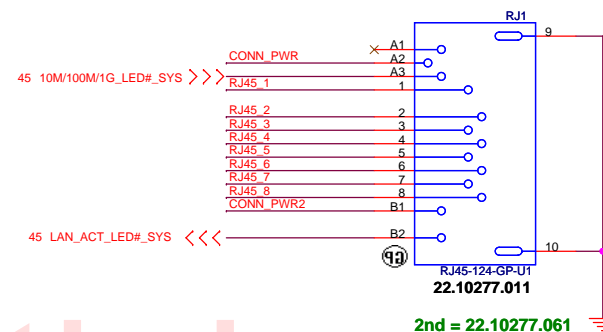


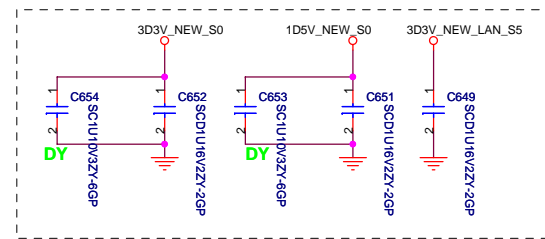
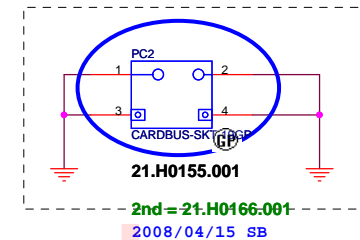
2008/04/11 SB
close to DB_CN2





LAN Connector





PCMCIA Socket

Cardbus I/F

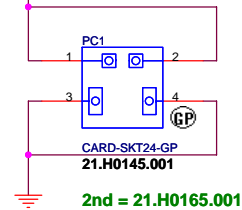
CBB_D[15..0] <<>> CBB_D[15..0] 30
CBB_A[25..0] <<>> CBB_A[25..0] 30

CBB_IORD# 30
CBB_IOWR# 30
CBB_OE# 30
CBB_WE# 30
CBB_REG# 30
CBB_RDY 30
CBB_WP 30
CBB_RESET# 30
CBB_WAIT# 30
CBB_INPACK# 30

CBB_CE1# 30
CBB_CE2# 30

CBB_CD1# 31
CBB_CD2# 31
CBB_VS1# 31
CBB_VS2# 31
CBB_BVD1# 31

PCMCIA-T/R, Frame



CARD-SKT24-GP

21.H0145.001

2nd = 21.H0165.001

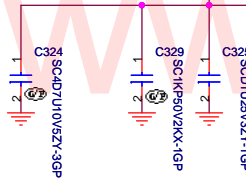
CARDBUS68P-26GP

62.10024.951

2nd = 62.10024.921

C344
SCD01U16V2KX-3GP
DY

VCC_ASKT_S0



DY

DY

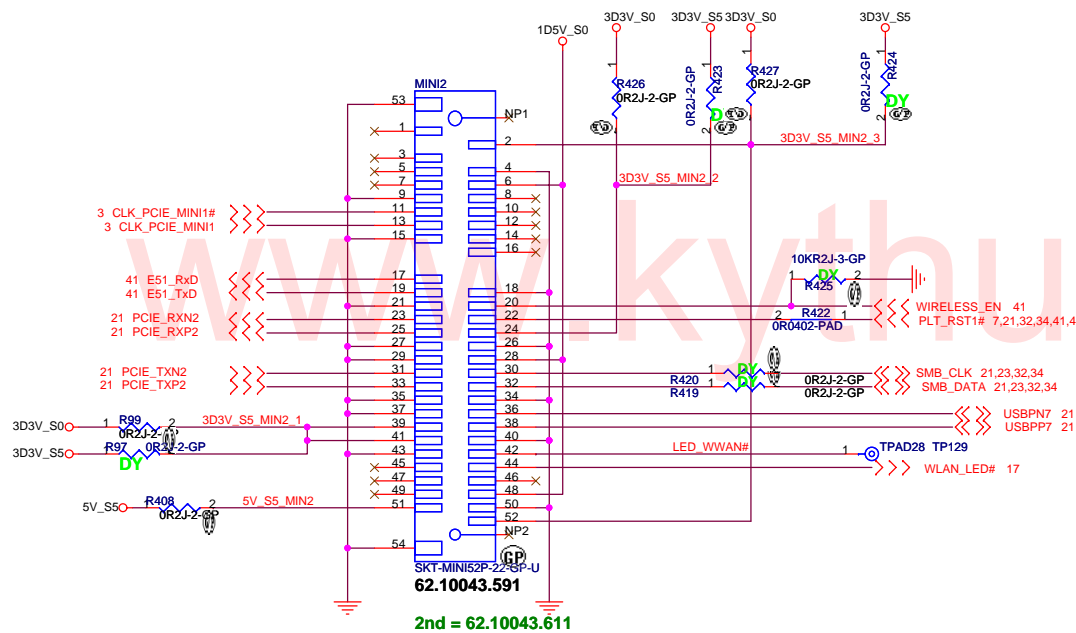
CBB_A16

Place close to pin 19.

C330
DUMMY-C2

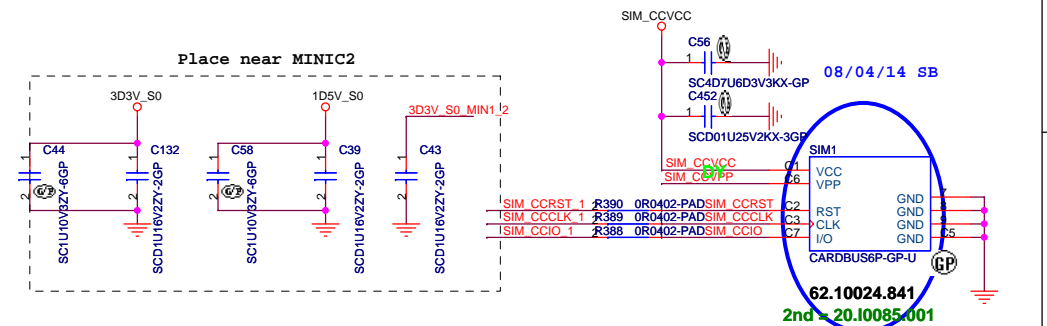
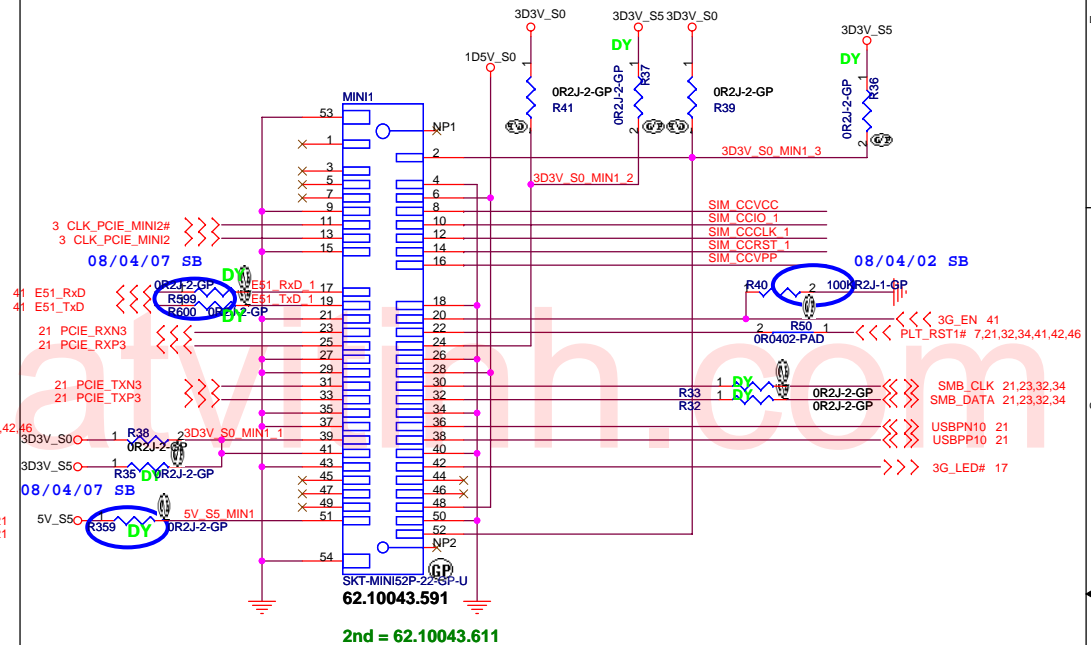
Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

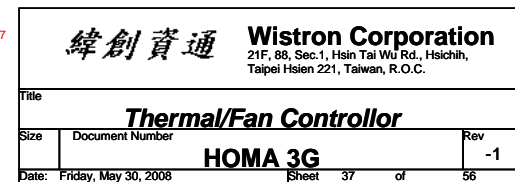
Mini Card Connector(WLAN)

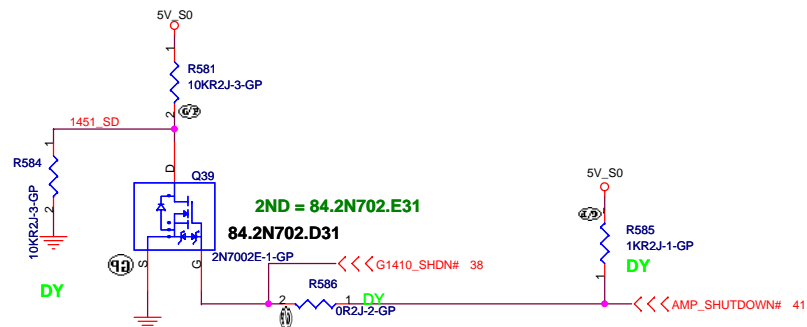
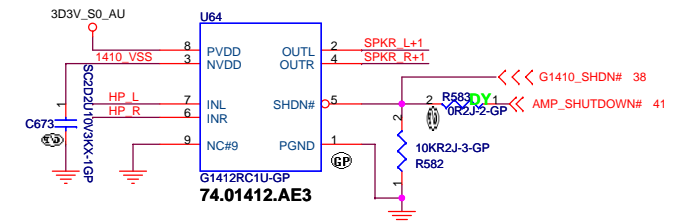
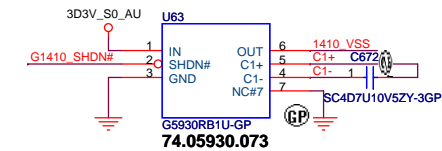
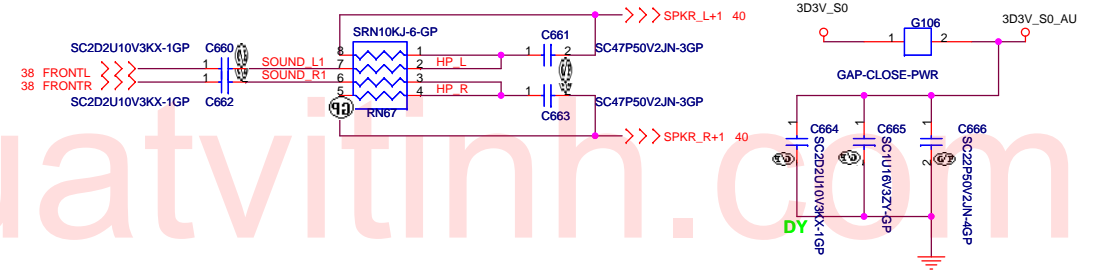
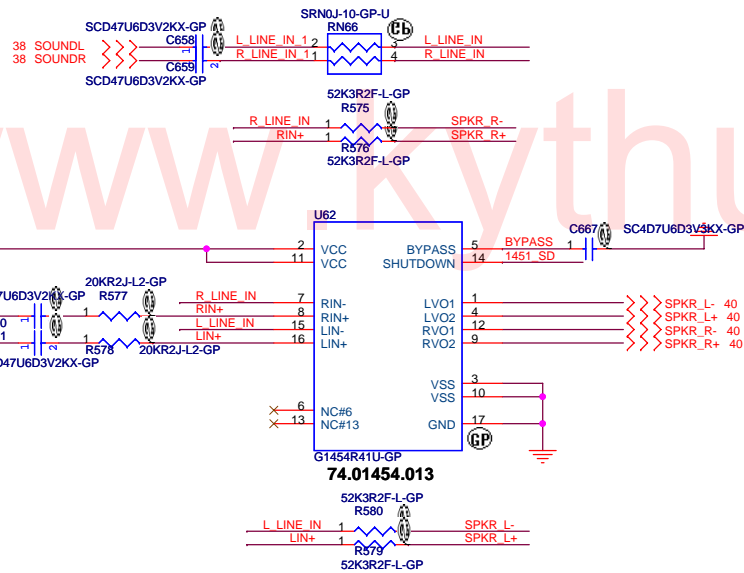


Mini Card Connector(Robson2 and 3G)

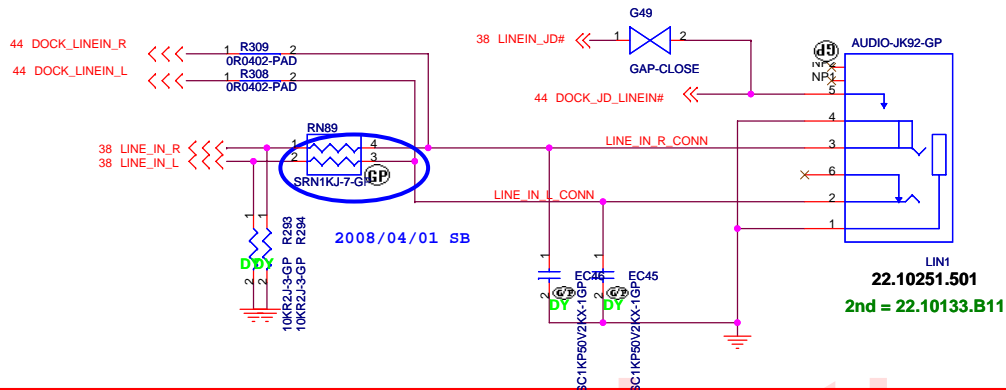
Support debug-card



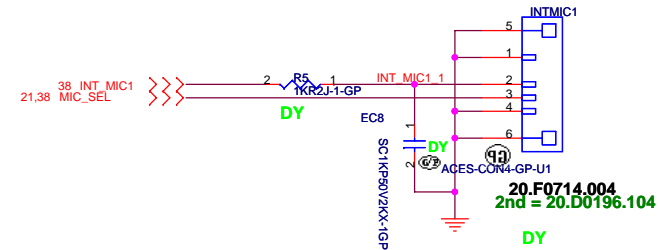




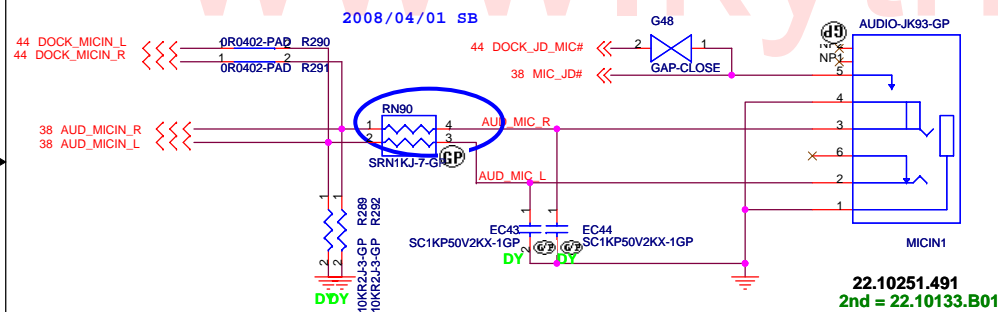
LINE IN



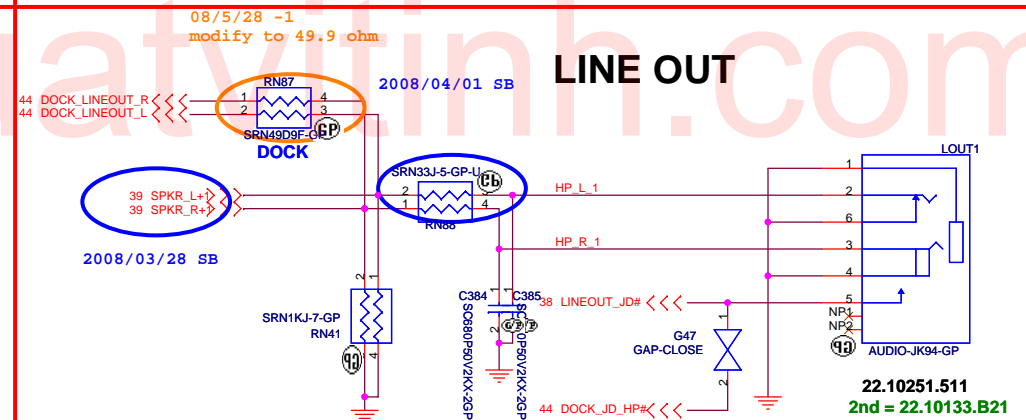
Internal Microphone



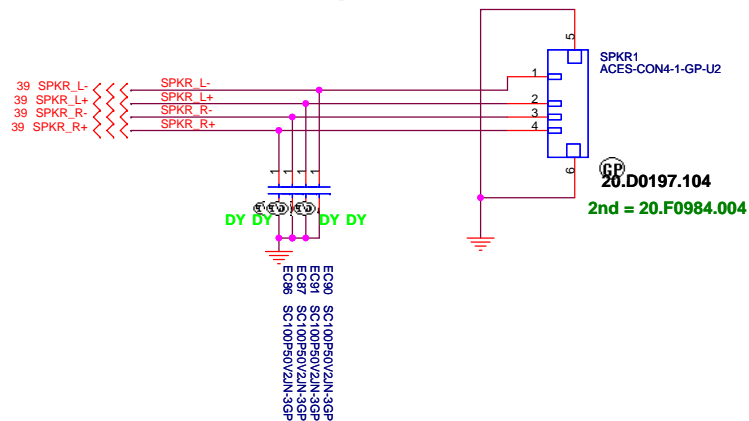
MIC IN



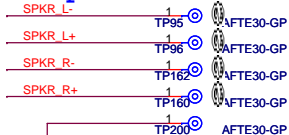
LINE OUT



Internal Speaker



SPKR1 Conn. Test Point keep on connector side



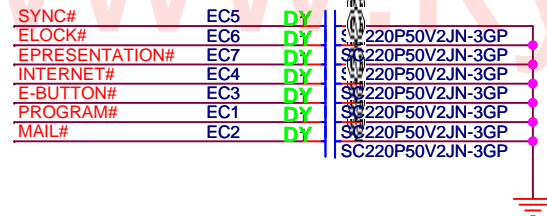
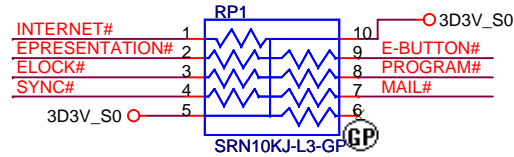
INTMIC1 Conn. Test Point keep on connector side



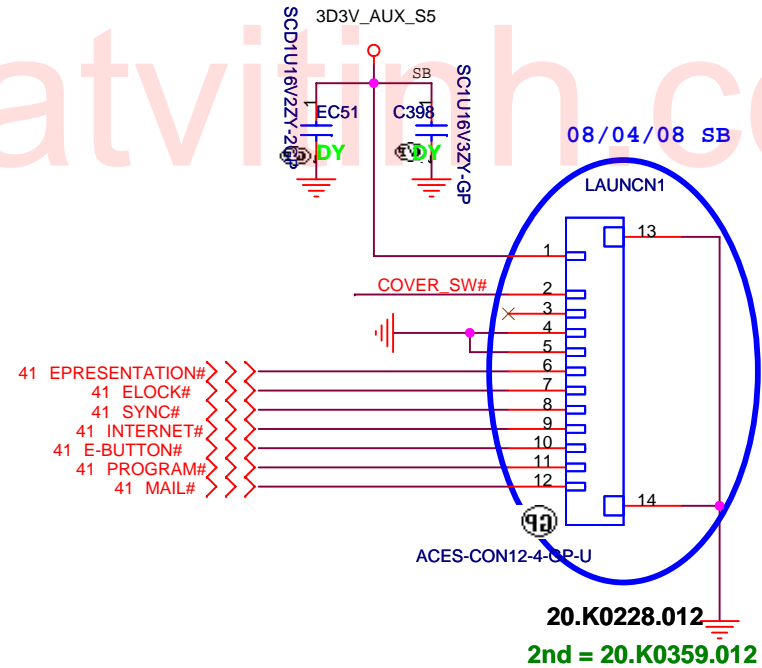
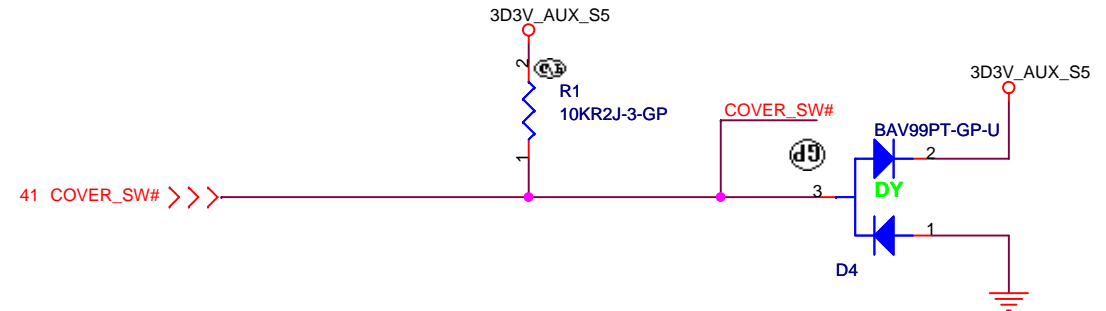
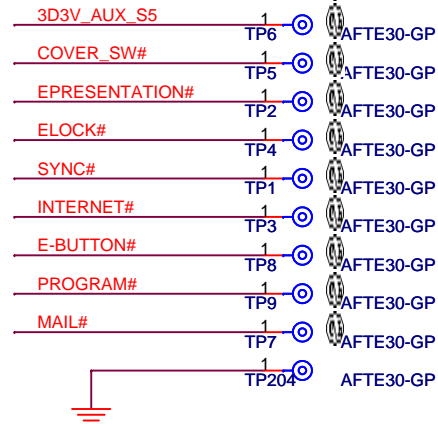
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO JACK		
Size	Document Number	Rev
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Cover Up Switch

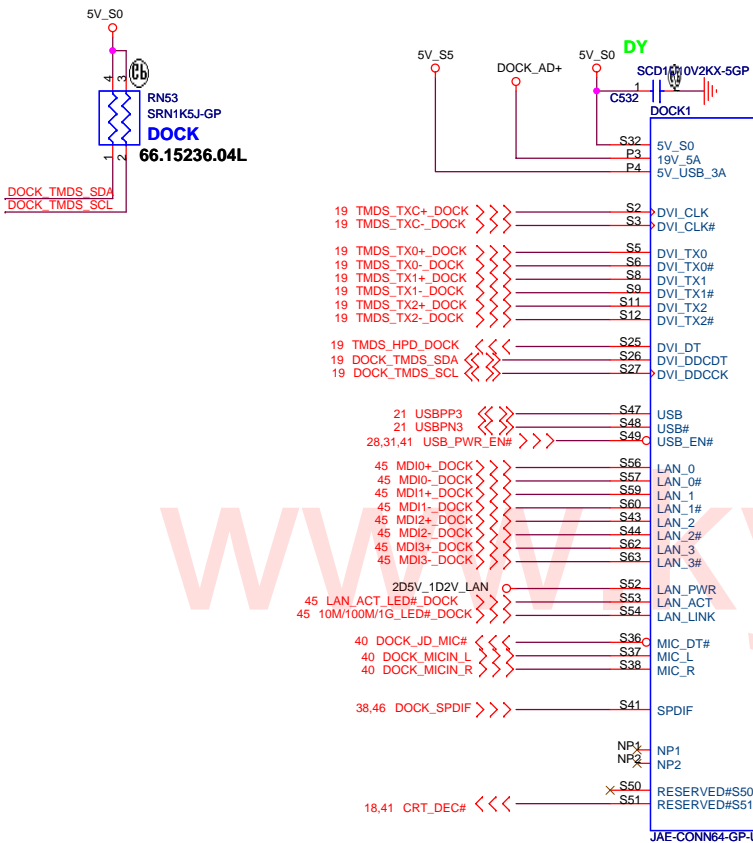


LAUNCH Conn. Test Point
keep on conector side



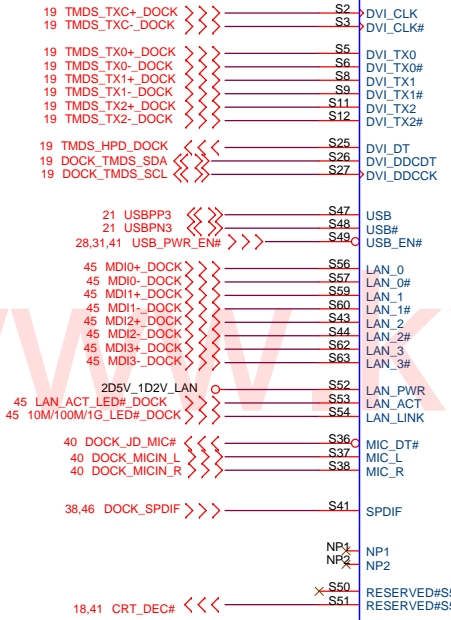
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Title LAUNCH		
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DOCK TMD5_SDA
DOCK TMD5_SCL

66.15236.04L



20.F1257.001

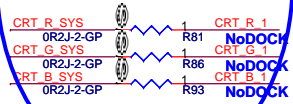
DOCK

2008/04/01 SB

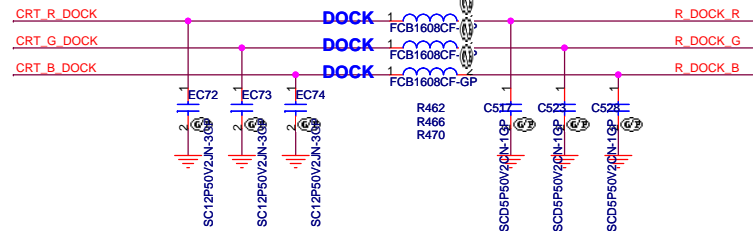


DOCK

2008/04/11 SB



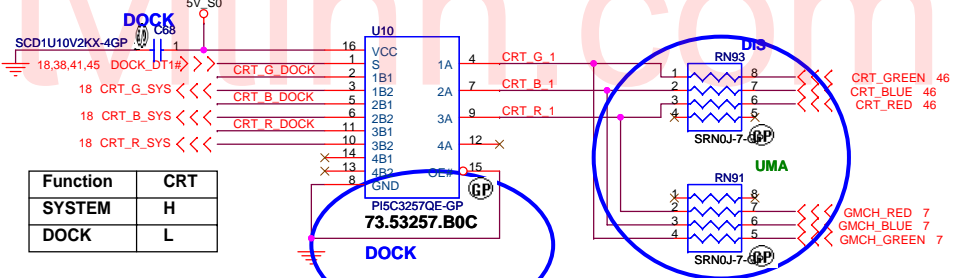
NoDOCK
NoDOCK
NoDOCK



68.00230.021
68.00230.021
68.00230.021

DOCKDOCKDOCK

CRT SWITCH

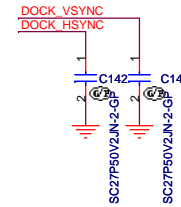


Function	CRT
SYSTEM	H
DOCK	L

2nd = 73.03257.A07

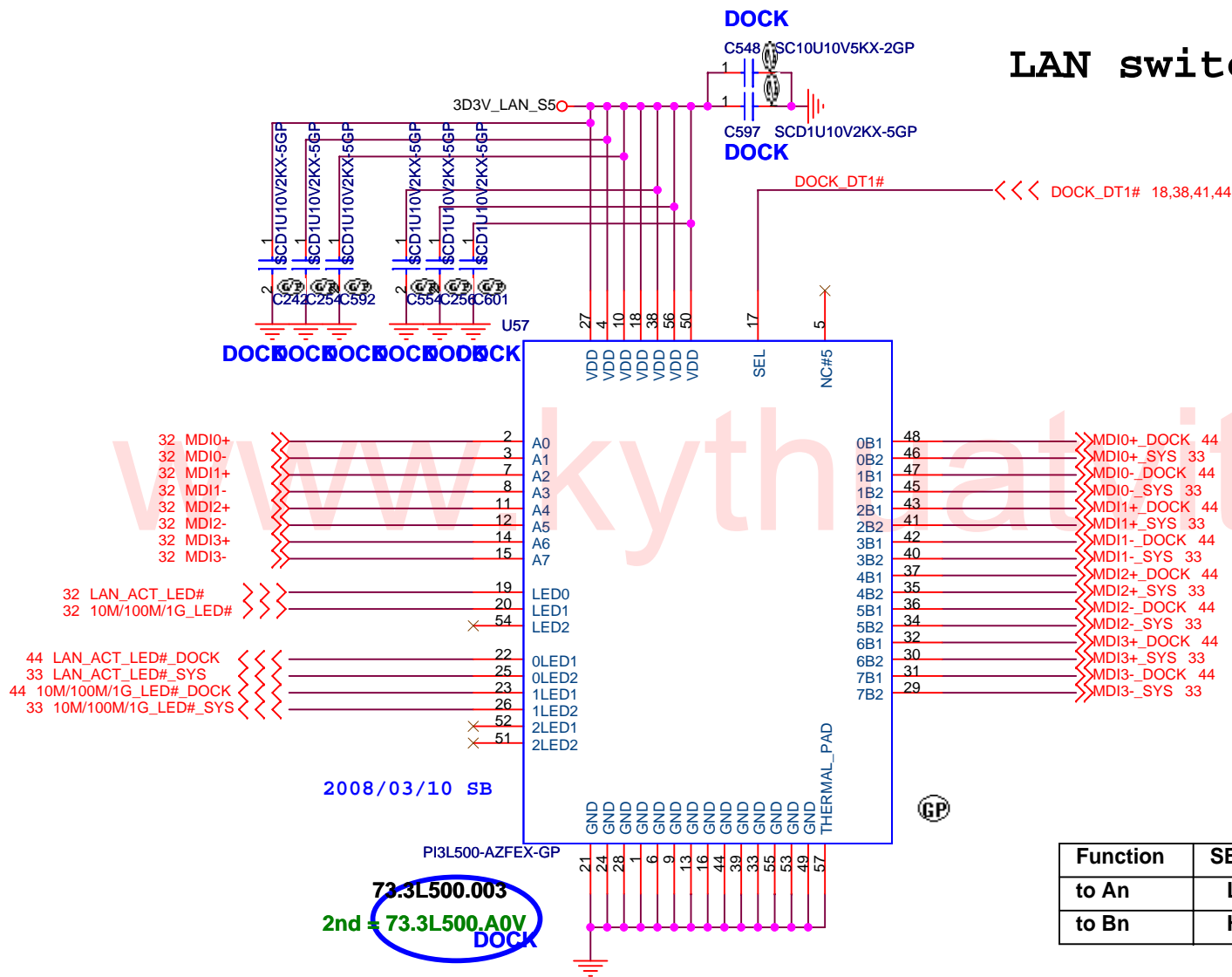
2008/03/13 SB

2008/04/01 SB

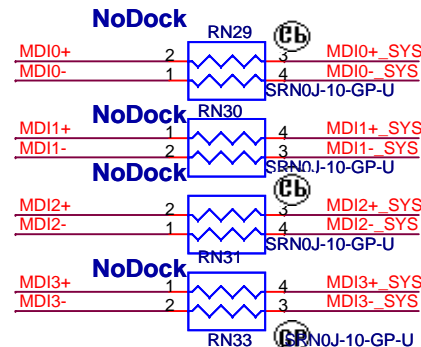
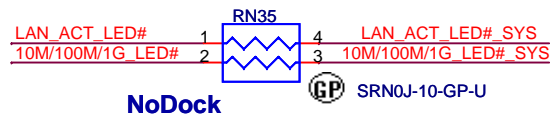


DOCKDOCK

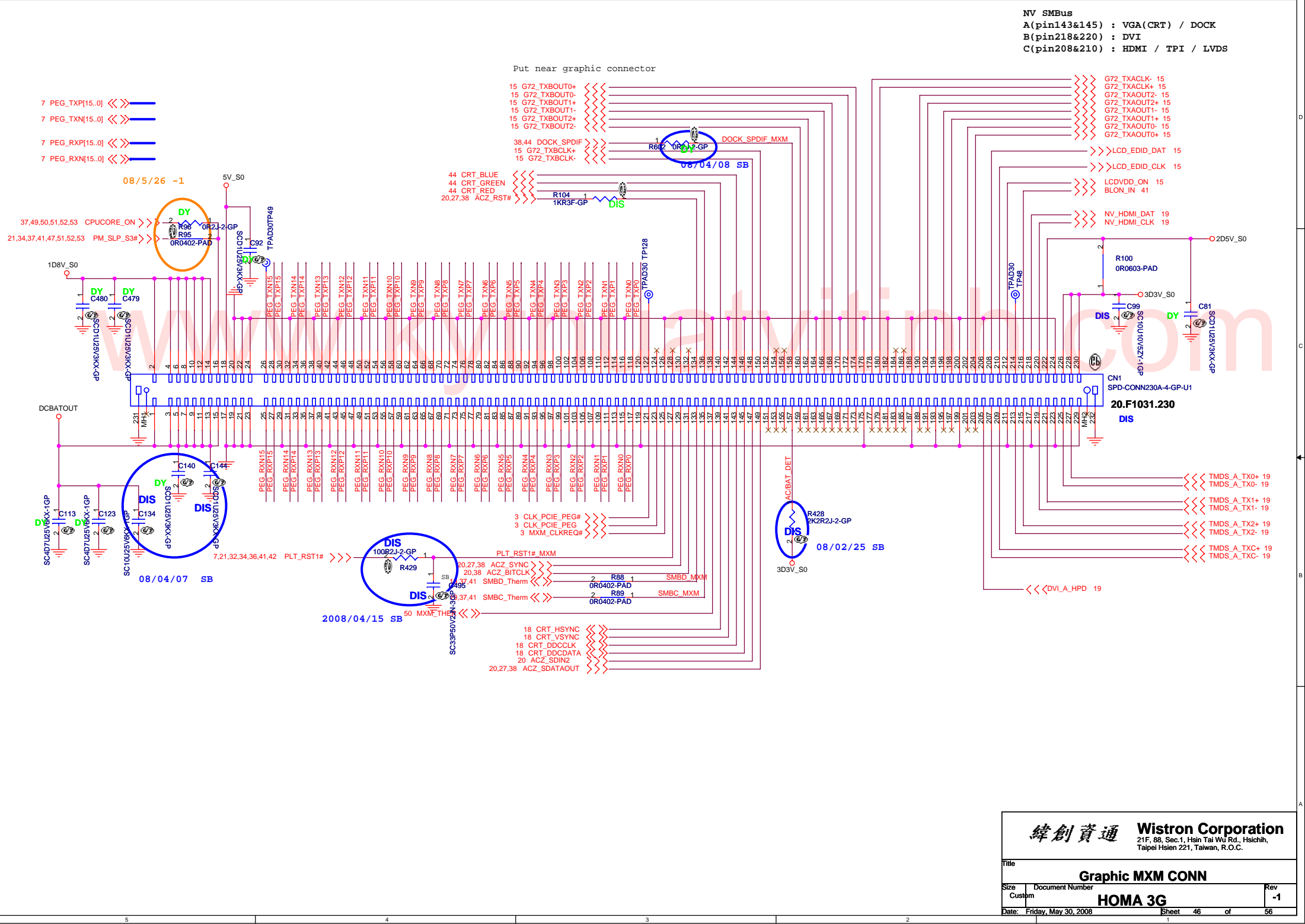
LAN switch



Function	SEL	
to An	L	DOCK
to Bn	H	SYSTEM



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Title EASY PORT4 (2/2)	
Size A4	Document Number HOMA 3G
Date: Friday, May 30, 2008	
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Rev -1	

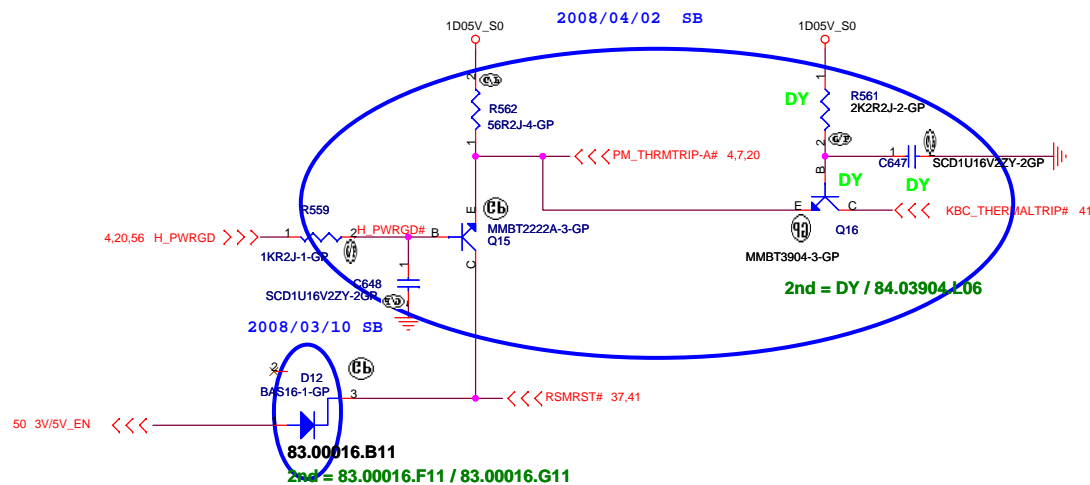


NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

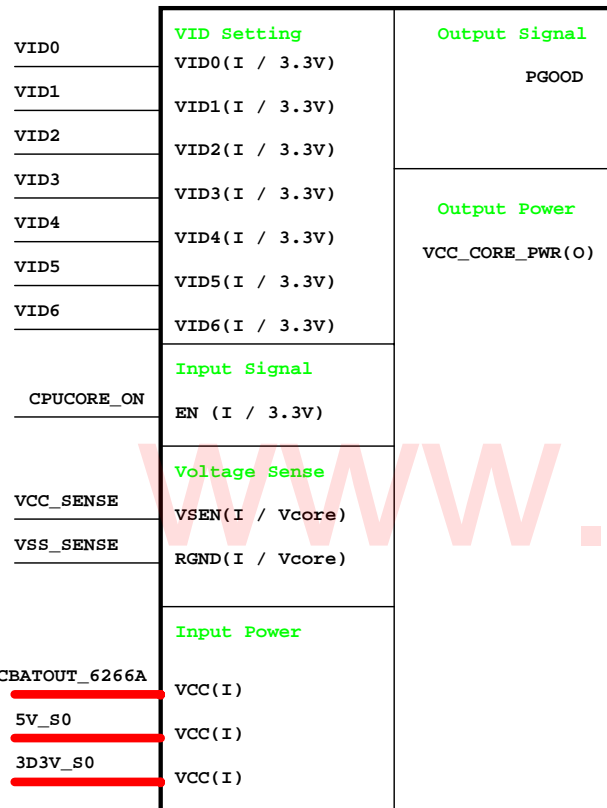
3D3V_AUX_S5



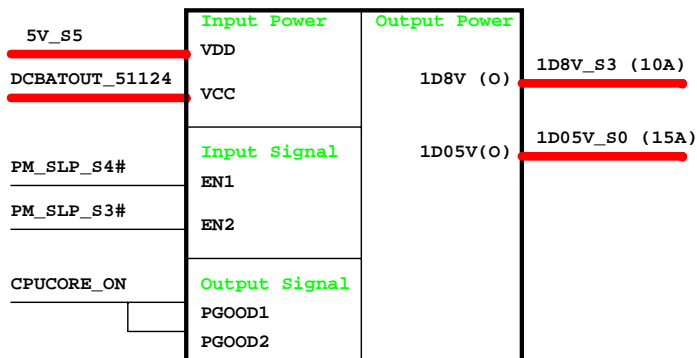
2008/03/10 SB



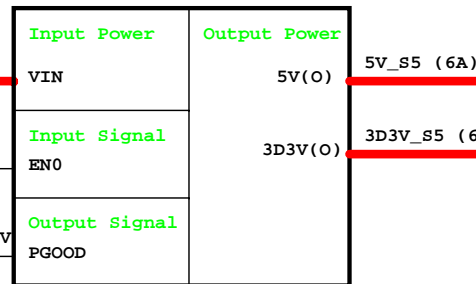
CPU_CORE
ISL6266A



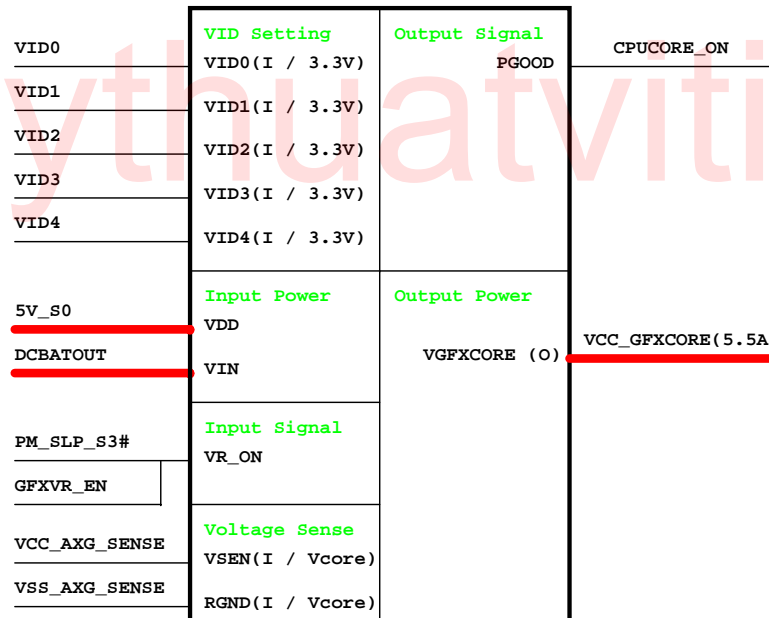
TPS51124
1D8V/1D05V



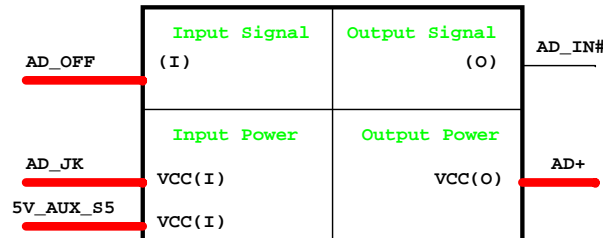
TPS51125
5V/3D3V



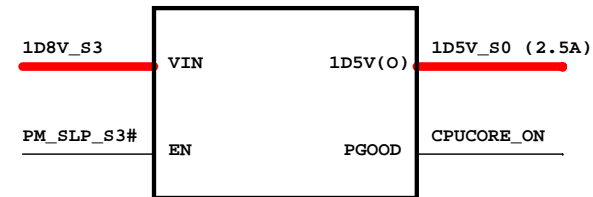
GFX_CORE
ISL6263A



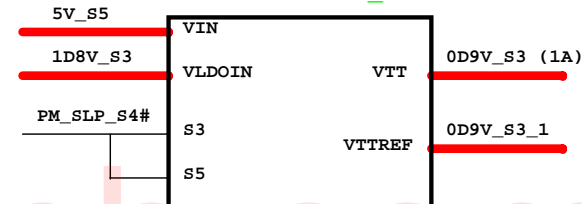
Adapter



RT9018A
1D5V_S0



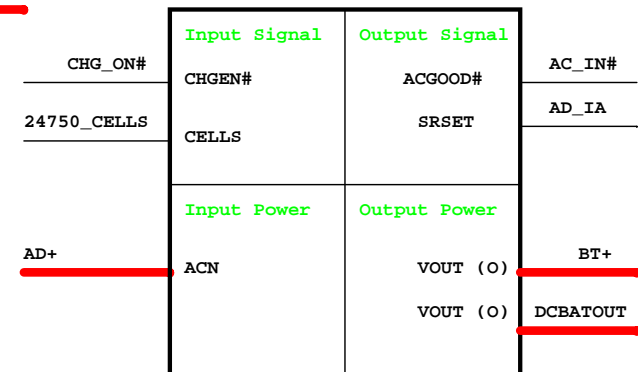
RT9026 0D9V_S0



G9131 2D5V_S0

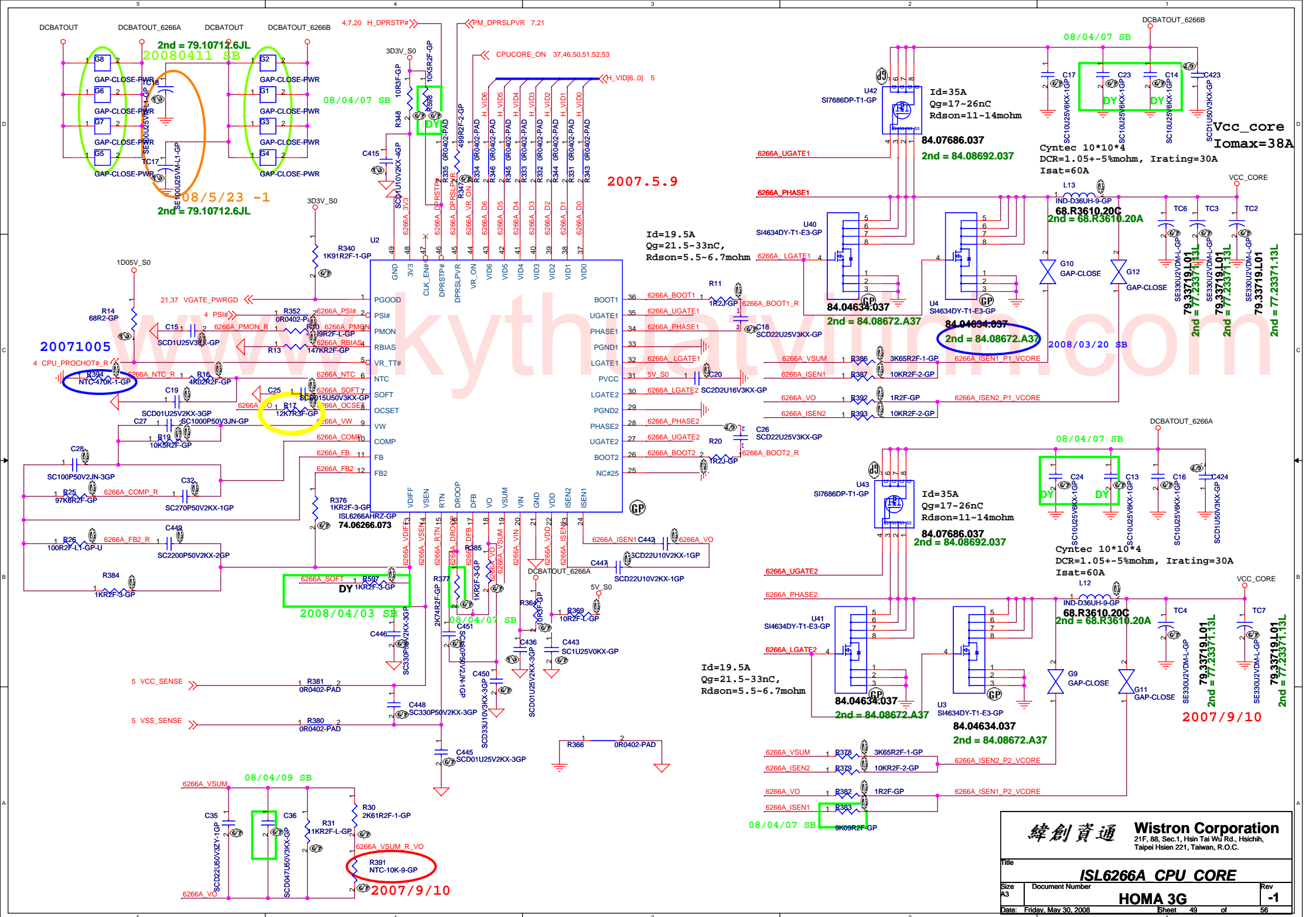


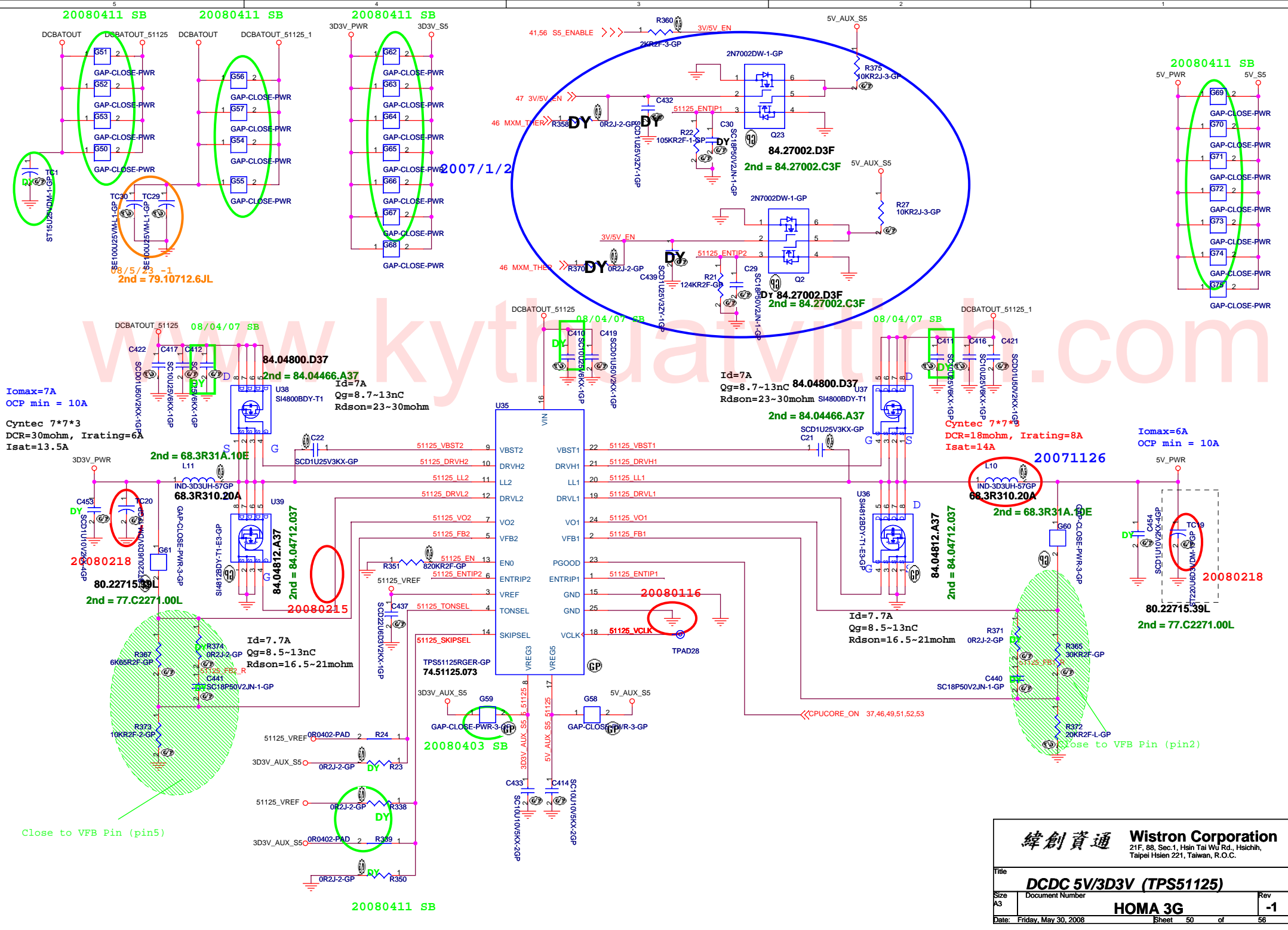
Charger BQ24750

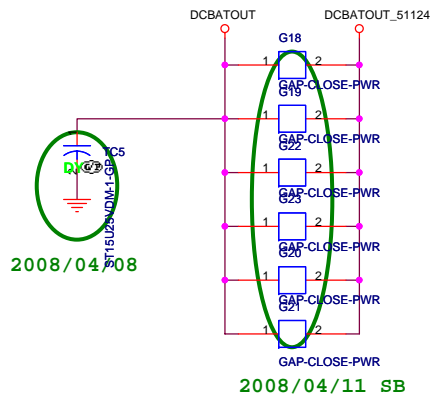


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Title			Power Block Diagram	
Size B	Document Number	HOMA 3G		Rev -1
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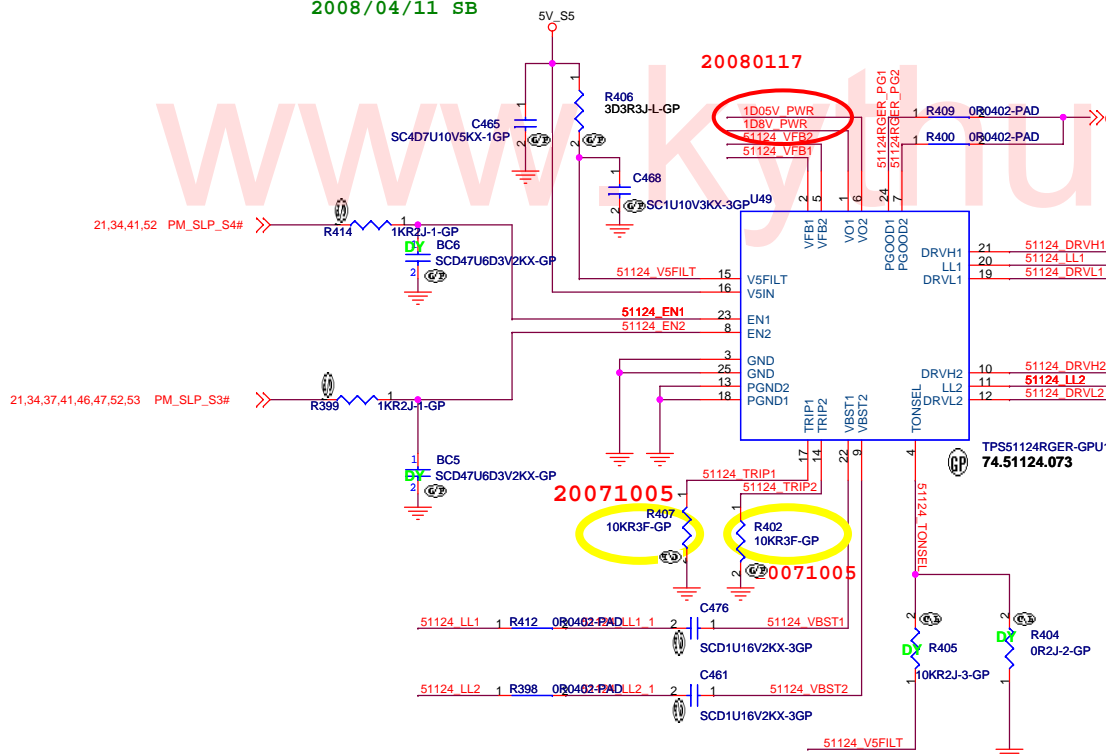
$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

2008/04/11 SB

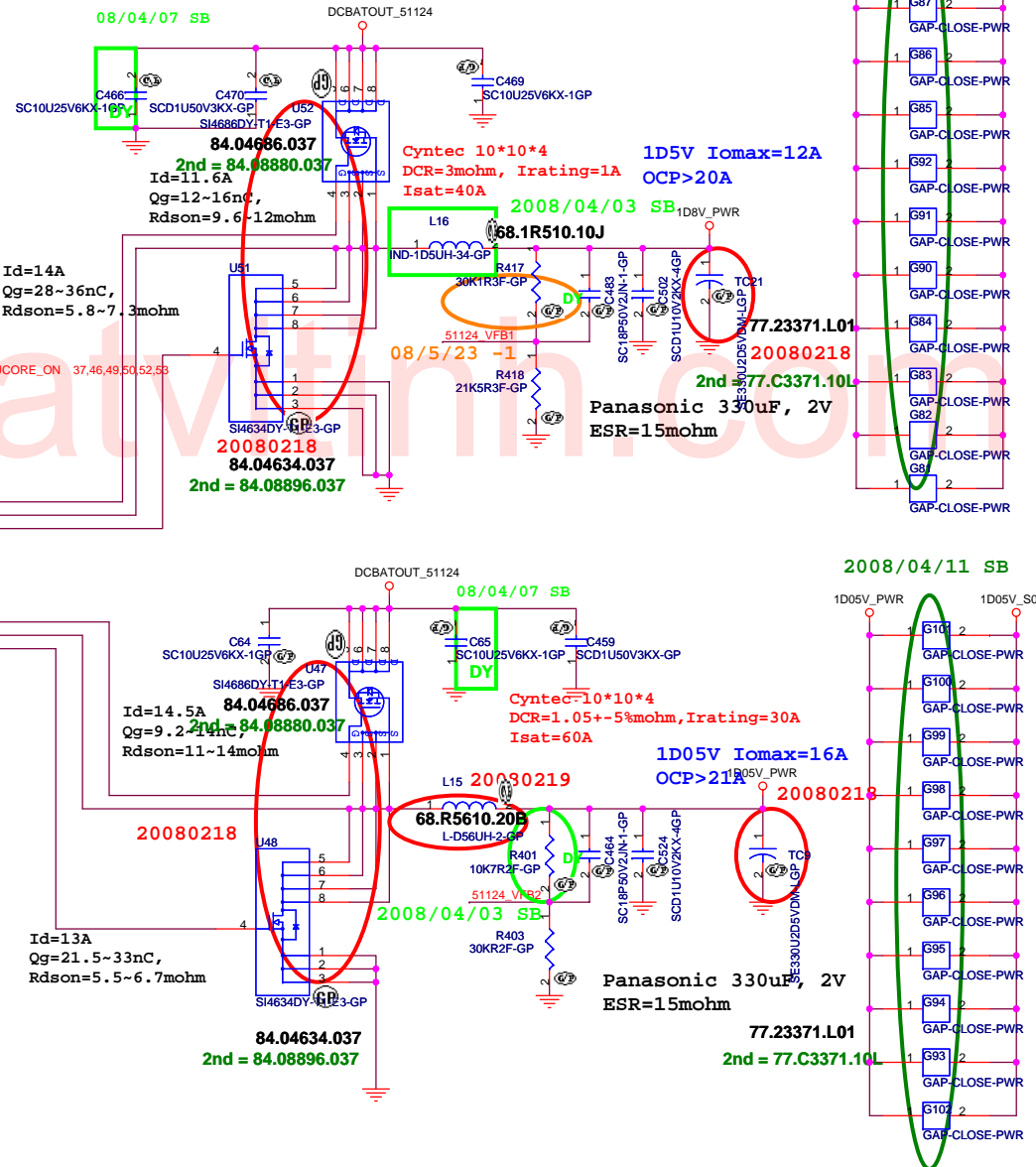
20080117



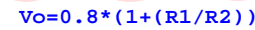
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$$V_{out} = 0.758V * (R1 + R2) / R2 \quad \text{--> PWM mode}$$

$$V_{out} = 0.764V * (R1 + R2) / R2 \quad \text{--> Skip Mode}$$

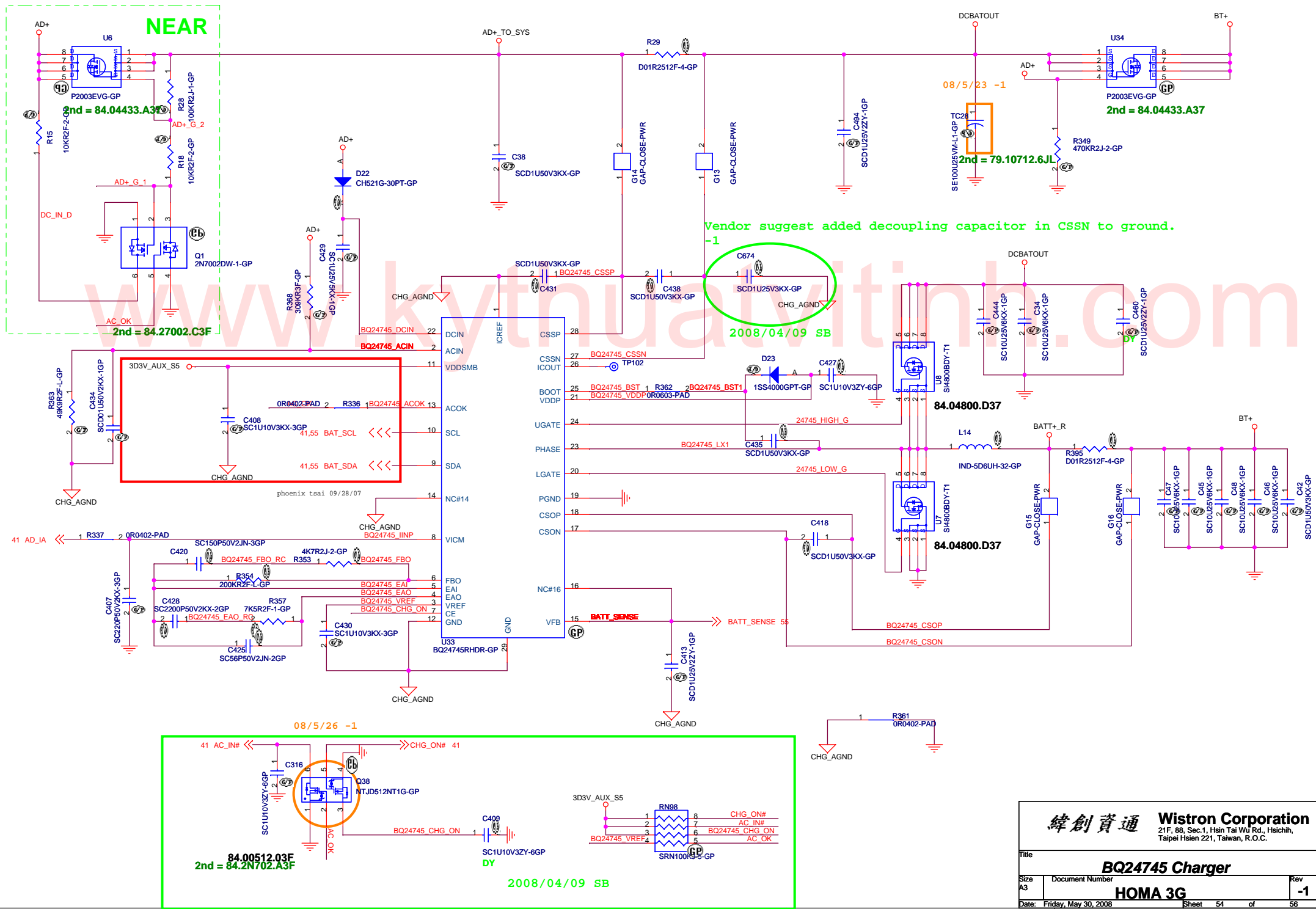


20071010



$I_{\text{max}} = 1.2 \text{ A}$
 $\text{OCP} > 2 \text{ A}$



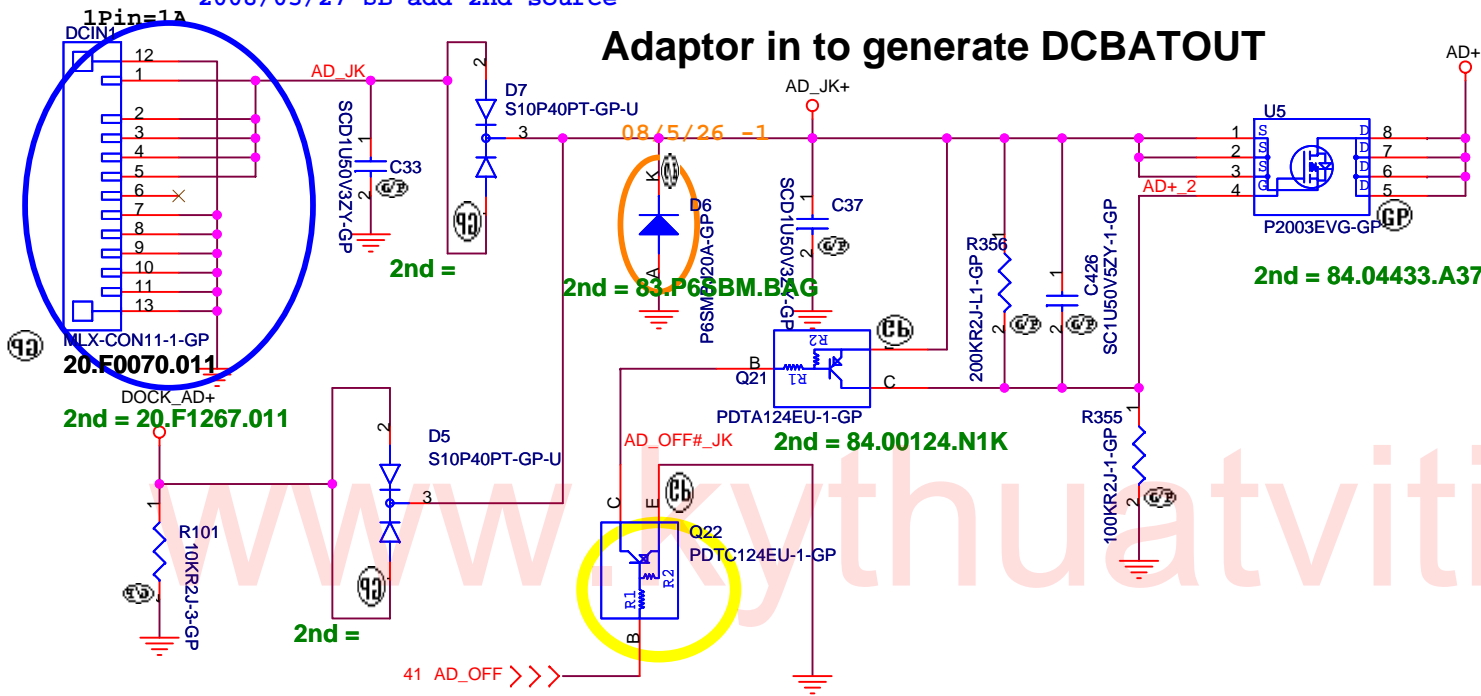


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Title			BQ24745 Charger	
Size	Document Number	Rev		
A3		HOMA 3G		-1
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2008/03/27 SB add 2nd source

Adaptor in to generate DCBATOUT



MAIN BATTERY CONNECTOR

